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Rakesh Ramachandran

Ultra-high Efficiency DC-DC Converter using GaN Devices

PhD thesis, August 2016

SDU Electrical Engineering
The Maersk Mc-Kinney Møller Institute

Ultra-high Efficiency DC-DC Converter using GaN Devices

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Preface

This thesis is submitted in partial fulfilment of the requirements for obtaining the PhD degree at the Faculty of Engineering, University of Southern Denmark. The research work was carried out during the period from September 2013 until August 2016 and was supervised by Associate Professor Morten Nymand at the University of Southern Denmark. This work was supported by the Danish National Advanced Technology Foundation under Intelligent Efficient Power Electronics (IEPE). IEPE is a strategic research center between industries and universities in Denmark. The collaboration is between various Danish universities, which include Aalborg University, Technical University of Denmark and University of Southern Denmark with the industrial partners Danfoss A/S, Grundfos A/S, KK Wind Solutions and Vestas. The overall goal of IEPE is to produce cheaper and more reliable electronic devices, which will accelerate the transition to sustainable energy solutions.

Acknowledgement

At first, I would like to express my deep gratitude to my supervisor Dr. Morten Nymand for trusting me and giving me the opportunity to do my PhD thesis at the University of Southern Denmark (SDU). His knowledge, research attitude and advices are more valuable during my PhD studies and they will keep helping me in my future life.

I am very thankful to have a good working environment and would like to thank all my colleagues and friends at SDU. I would also like to give my special appreciation to all the former and present colleagues at the Maersk Mc-Kinney Moller Institute especially to Alireza Kouchaki, Farideh Javidi, Fazel Taeed, Ishtiyah Ahmed Makda, Karsten H. Andersen and Jacob Lykke Pedersen for all your support to finish this project.

My special thanks to Jesper Nielsen for helping me with PCB, magnetics and his great effort to realize the hardware prototypes of the converter.

It was a great pleasure to work with various partner universities and companies of IEPE. I would like to thank all the fellow members of IEPE for having interesting dialogues and discussions at various IEPE workshops and meetings.

I would also like to thank Professor Johann W. Kolar for giving me an opportunity to work as an Academic Guest at the Power Electronics System (PES) Group at Eidgenössische Technische Hochschule (ETH) Zürich, Switzerland during my PhD studies.

Finally, I would like to thank all my family members and friends, too numerous to name, for their encouragement and great support, without whom the successful completion of this thesis would not have been possible.

Odense, August 2016
Rakesh Ramachandran

Abstract

The demands for high efficiency dc-dc power converters are increasing day by day in various applications such as telecommunication, data-centers, electric vehicles and various renewable energy systems. Silicon (Si) has been used as the semiconductor material in majority of the power devices for many decades. However, the rate of improvement slowed as the silicon power materials asymptotically approached its theoretical bounds. Compared to Si, wideband gap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are promising semiconductors for power devices due to their superior material properties such as high temperature operation, high breakdown voltage and high frequency operation. Among wide band-gap devices, GaN has an enhanced mobility of electrons, compared to SiC, which helps in achieving smaller size for a given on-resistance and breakdown voltage. These superior properties of GaN devices can be utilized in power converters to make them more compact and highly efficient.

This thesis entitled “Ultra-high Efficiency DC-DC Converter using GaN devices” focuses on achieving ultra-high conversion efficiency in an isolated dc-dc converter by the optimal utilization of GaN devices. Simple replacement of Si or SiC devices with GaN devices in the converter will not give an expected increase in efficiency or any improvement in the performance of the converter. The use of GaN devices has defined another dimension in the design of power converters, which mainly deals with the PCB layout and the magnetics.

This thesis mainly covers the design and implementation of various high efficiency isolated dc-dc converters in the range of 1 to 2.5 kW of output power. Both hard-switched and soft-switched topologies in isolated dc-dc converters has been studied and realized in this thesis. Efficiency measurements from the hardware prototype of both the topologies are also presented in this thesis. Finally, the bidirectional operation of an optimized isolated dc-dc converter is presented. The optimized converter has achieved an ultra-high efficiency of 98.8% in both directions of power flow.

In chapter 2, literature review of various high efficiency isolated dc-dc converters is presented. An overview of properties of GaN devices and their usage in dc-dc converter is also included in this chapter. The utilization of GaN devices in isolated dc-dc converters for high power applications is scarcely available in literature.

In chapter 3, the design considerations and loss modelling for an isolated dc-dc forward converter is presented. The major contributions from this chapter are given below:

- A comprehensive analytical loss modeling for an isolated dc-dc forward converter is formulated.

- Output capacitive losses from the switching devices, which constitute the major portion of switching loss for an isolated dc-dc converter is estimated and presented.
- Experimental demonstration of high efficiency on a 1.7 kW isolated dc-dc GaN converter.

In chapter 4, the analysis of a phase shifted isolated converter using the magnetizing current of the transformer is presented. The major contributions from this chapter include:

- Soft switching in the devices can be achieved even at very low output power level using the magnetizing current of the transformer
- The deviation of peak efficiency point with the variation of magnetizing current is illustrated in this chapter.
- The measured maximum efficiency of a 1 kW phase shifted isolated GaN converter is 98.8%

In chapter 5, an optimized bidirectional isolated dc-dc converter is presented. A 2.4 kW isolated dc-dc converter is designed with optimizing the layout and the converter operation in both forward (buck mode) and backward directions (boost mode) are experimentally verified. The converter has achieved a maximum measured efficiency of 98.8% in both directions of power flow. The proposed converter also has a power density of 7 kW/liter at 50 kHz. The chapter also illustrates that with the optimization of layout the power density of the converter can be increased for a certain switching frequency.

Resumé

Kravene for højeffektive dc-dc konvertere er stigende dag for dag indenfor forskellige anvendelsesområder såsom telekommunikation, data centre, elektriske køretøjer og forskellige vedvarende energisystemer. Silicium (Si) har igennem de sidste årtier været det foretrukne materiale til halvlederkomponenter indenfor power elektronik. I dag går udviklingen af power silicium komponenter langsomt, idet den teoretiske grænse for yderlige forbedringer er ved at være nået. Sammenlignet med Silicium er wideband gap komponenter såsom Siliciumkarbid (SiC) og GalliumNitrid (GaN) meget lovende som power elektronikkomponenter pga. deres overlegne materialeegenskaber som f.eks. høj arbejdstemperatur, høj robusthed overfor spændings overslag, og de kan drives ved en høj frekvens. Bland wide band gap komponenterne er GaN specielt god til at overføre elektroner hvilket muliggør en fysisk lille komponent for en given ledemodstand. Disse overlegne egenskaber gør at GaN er et oplagt valg i power konvertere for at gøre dem mere kompakte og effektive.

Denne afhandling med titlen ”Ultra-high Efficiency DC-DC Converter using GaN devices” fokuserer på at opnå ultra høj effektivitet i isolerede dc-dc konverter ved optimalt at udnytte GaN komponenter og dens egenskaber. Simpel udskiftning af Si eller SiC komponenter til GaN, vil som udgangspunkt ikke give en øget effektivitet af konverteren. Brugen af GaN kræver et andet PCB layout samt design af de magnetiske komponenter.

Denne afhandling omhandler primært design og implementering af forskellige højeffektive isolerede dc-dc power konvertere, med en udgangseffekt på 1 – 2,5kW. Både isolerede dc-dc konvertere med hard-switching og soft-switching topologier er blevet studeret og realiseret. Effektivitetsmålinger fra de konstruerede hard og soft-switching prototyper bliver præsenteret i afhandlingen. Sidst men ikke mindst, bliver der præsenteret en optimeret bi-directional isoleret dc-dc konverter. Den optimerede konverter opnåede en ultra høj effektivitet på 98,8% gældende for effekten i begge retninger.

I kapitel 2, bliver litteraturen af forskellige højeffektive isolerede dc-dc konvertere gennemgået. Derudover giver kapitlet et overblik over GaN komponenter og deres anvendelse i dc-dc konvertere, da GaN komponenter i isolerede dc-dc konvertere til høj effekt er ikke udbredt beskrevet i litteraturen.

I kapitel 3, bliver designovervejelser og effekttabsmodellering for en isoleret dc-dc konverter præsenteret. Hovedemnerne i kapitlet er:

- En gennemgående analytisk model for effekttabet i en isoleret dc-dc konverter
- Udgangskapacitetstab fra de switchende komponenter, som bidrager til hoveddelen af switch tabene i en isoleret dc-dc konverter, bliver vurderet og præsenteret.

- Eksperimentel demonstration af en højeffektiv 1,7kW isoleret dc-dc GaN konverter

I Kapitel 4, bliver analysen af en phase shifted isoleret konverter, som benytter magnetiseringsstrømmen fra transformatoren, præsenteret.

Hovedemnerne i kapitlet er:

- Det vises at soft-switching kan opnås selv ved lav effekt ved at bruge magnetiseringsstrømmen fra transformeren.
- Det ændrede toppunkt af effektivitetskurven som funktion af magnetiseringsstrømmen er illustreret i dette kapitel.
- Den målte maksimale effektivitet på en 1kW phase shifted isoleret GaN konverter er 98,8%

I kapitel 5, bliver en optimeret bi-direktional isoleret dc-dc konverter præsenteret. En 2,4kW isoleret dc-dc konverter bliver designet med et optimeret print layout, og afprøvet i begge retninger, (Buck og Boost mode). Konverteren opnåede en maksimalt målt effektivitet på 98,8% i begge retninger. Konverteren har en energitæthed (power density) på 7kW/liter ved 50kHz. Dette kapitel illustrerer at med optimering af print layoutet, kan energitætheden øges, for en specifik switching frekvens.

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Abbreviations

WBG	Wide Band Gap materials/devices
Si	Silicon
GaN	Gallium Nitride
SiC	Silicon Carbide
SJ	Super Junction technology
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
FET	Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
HEMT	High Electron Mobility Transistor
DAB	Dual Active Bridge
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
IR	Infra-Red
PCB	Printed Circuit Board
IGSE	Improved Generalized Steinmetz Equation
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
PWM	Pulse Width Modulation
ppm	parts per million
RMS	Root Mean Square
HVS	High Voltage Side
LVS	Low Voltage Side
ESR	Equivalent Series Resistance
MLCC	Multi-Layer Ceramic Capacitor

Nomenclature

μ	Electron mobility
E_g	Energy gap
g_m	Trans-conductance
f_T	Frequency response (cut-off frequency)
$R_{(ON)}$	On-resistance
L_m	Magnetizing inductance
L_{lk}	Leakage inductance
F_R	Resistance factor
R_{ac}	ac resistance
R_{dc}	dc resistance
n	Transformer turns ratio
f_{sw}	Converter switching frequency
f_L	Inductor switching frequency
T_s	Converter time period
T_L	Inductor time period
N_p	No. of turns in the primary winding
N_s	No. of turns in the secondary winding
h	Height of conductor
h_p	Height of p^{th} winding portion
h_Δ	Height of primary-secondary intersection
μ_0	Permeability of free space
δ	Penetration depth in material
l_w	Mean turn length
b_w	Breadth of winding
m	Number of layers in winding portion
M	Number of primary-secondary intersections
D	Duty cycle
D_L	Inductor duty cycle
C_{iss}	Input capacitance
C_{rss}	Reverse transfer capacitance
C_{oss}	Output capacitance
C_{gd}	Gate-to-drain capacitance
C_{gs}	Gate-to-source capacitance
C_{ds}	Drain-to-source capacitance
V_d	Gate drive voltage
Q_G	Gate charge

1. Introduction

1.1. Scope

The scope of this thesis entitled “Ultra-high Efficiency DC-DC Converter using GaN Devices” is to present the results achieved during the PhD project, which has been carried out by the author during the period from September 2013 to August 2016. Most of the research outcomes of this project have already been published/submitted in various peer reviewed conferences and journals. These scientific papers forms an integral part of this thesis and are included in the appendix. The objective of this dissemination is to give a coherent and complete overview of the research work carried out by the author during his PhD studies.

1.2. Background and Motivation

The most significant task in a power supply design is the reduction of power loss and hence increasing the efficiency of power converters. By reducing the power loss, the size of the heatsink and magnetics can be reduced. This consecutively reduces the size of the whole converter and makes them more compact.

The trade-off between efficiency, power density, cost and size of the converter cannot be easily defined because it is highly dependent on the applications and market requirements. The power density of the converter is inversely proportional to the size of the passive components such as transformer, inductors and capacitors. By increasing the switching frequency, the power density can be increased but due to the increase of switching frequency, the switching losses can increase and thus efficiency of the converter decreases. Even though switching losses can be minimized by resonant or various soft switching topologies, they becomes more and more complicated by the introduction of supplementary active or passive power components.

Silicon has been used as the major power semiconductor materials in power devices for many decades [1]. In recent years, wide band gap semiconductors were introduced into the power semiconductor market. Among various wide band gap devices, SiC and GaN devices become more attractive in power converters due to their superior material properties compared to Si devices [2]-[4]. Various studies on SiC as power devices have been widely documented in the recent literature [10], [11]. However, there were only a few studies on GaN devices for high power converters (kW converters) [11]-[14] were available. This research work is carried out to study and verify the optimal application of GaN devices in an isolated dc-dc converter to achieve an ultra-high efficiency and to make them more compact. The only commercially available high voltage GaN devices at the starting of this project were 200V GaN devices from Efficient Power Conversion (EPC). Today GaN devices for a breakdown voltage of up to 650V are available. Nowadays, GaN FETs are available from manufactures such as EPC, GaN

systems and Panasonic, which provides enhancement mode GaN FETs, while Infineon, Transphorm and GaN systems provides cascode GaN FETs.

In recent years, significant research interest has been noticed in improving the conversion efficiency of an isolated dc-dc converter [15]-[20]. These power converters are essential in many applications such as telecom industries, datacenters and electric vehicles. The majority of power converters are unidirectional with the power being supplied from source to load. Many applications like motor drives, uninterruptable power supplies, renewable energy sources, battery chargers require the additional exchange of energy from load to source. It would be highly desirable to have such power converters with bidirectional power transfer properties. Fig. 1.1 shows the various applications of isolated dc-dc converters.

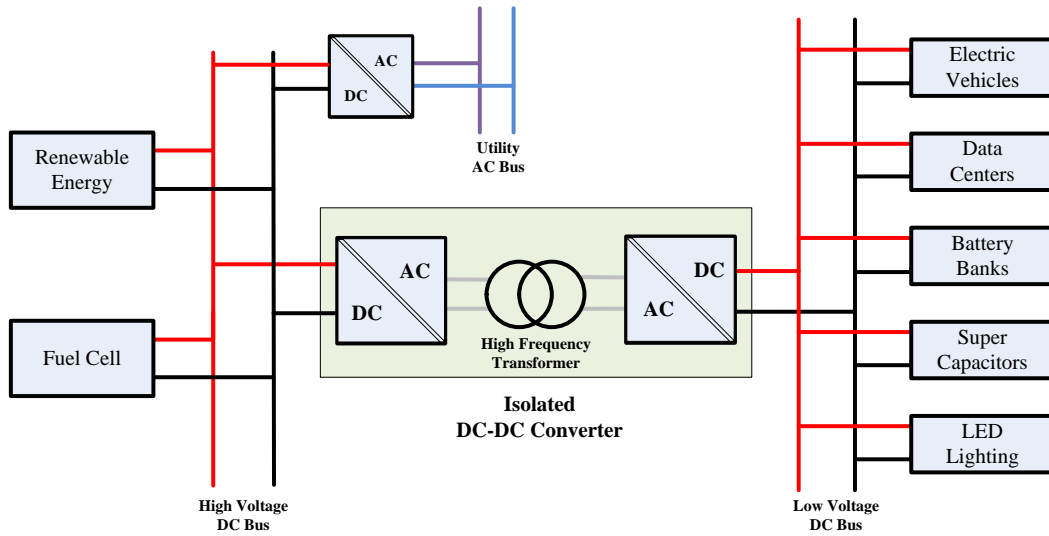


Fig. 1.1. Application of isolated dc-dc converters

Various converter topologies and implementations are proposed to achieve ultra-high efficiency in isolated dc-dc converters [7], [15]-[20]. Most of the isolated converters use zero voltage switching (ZVS) for efficiency improvement. To select between hard or soft switching topologies, first the switching losses in the converter should be analyzed before the implementation, to have an optimized converter with highest conversion efficiency.

Isolated dc-dc converters with a power range of 1 to 5 kW having a maximum efficiency of around 98% are being discussed in literature [18], [19], [22], [31], and [36]. It is, therefore, a very challenging task to improve the efficiency of these converters even further, but usage of wide band gap devices along with proper magnetic design can improve the efficiency of such converters further. An increase in switching frequency helps in minimizing the filter size and magnetics. A major advantage of wide band-gap devices is their low output charge, which will reduce the switching losses compared to Si devices. As the total power loss in the converter reduces, the size of the heat sink requirement reduces, which in turn reduces the overall size of

the converter. Thus, a compact and ultra-high efficiency converter can be realized. In other words, for a particular switching frequency, by reducing the losses in a converter, more power can be transferred to the load, thereby increasing the power density, without scarifying the performance of the converter.

1.3. Project Objectives

The primary objective of this research work is to demonstrate the highest possible conversion efficiency in an isolated dc-dc converter. The project focuses on the analysis and application of GaN devices for an isolated dc-dc converter. A complete analytical loss modelling of the converter is also included as a part of this research work.

The second major objective is to study and realize an optimized bidirectional dc-dc converter to achieve the highest possible conversion efficiency, using the same power components in both directions of power flow.

1.4. Specifications

At the start of this project, the highest breakdown voltage of commercially available GaN FETs was only 200V. Since the main objective of this project is to realize an ultra-high efficiency isolated dc-dc converter utilizing GaN devices, the high voltage side has been defined as 130V and the low voltage side has been selected as 50V. 200V GaN devices are used at the high voltage side and 100V devices at the low voltage side. Various isolated dc-dc converters having power range of 1 to 2.5 kW are presented in this thesis. As the efficiency of the converter increases, the power loss associated with them decreases, which in turn reduces the heat sink requirement. This will reduce the overall size of the converter; hence, a compact converter can be realized. To achieve ultra-high conversion efficiency in high power converters, the switching frequency has to be reduced. Due to high current switching in high power converters, and considering factors such as penetration depth, copper fill-factor, and circuit parasitics, the switching frequency has been optimally selected as 50 kHz.

1.5. Thesis Structure

The structure of the thesis is presented as a flow chart in Fig. 1.2. Chapter 2 includes the literature review of dc-dc converters using GaN devices. This chapter also presents the literature review on various isolated dc-dc converters, which have achieved the highest conversion efficiency. Chapter 3 presents the loss model for an isolated dc-dc buck converter. The chapter also includes design and analysis of high efficiency magnetics. Hardware prototyping of a 1.7 kW isolated dc-dc buck converter is also presented in this chapter. The design and analysis of a phase-shifted isolated dc-dc converter is presented in chapter 4. Zero voltage switching in the phase-shifted converter is achieved using the magnetizing current of the transformer. This

allows the soft switching of the devices even at very low output power. Chapter 5 presents an optimized 2.4 kW bidirectional isolated dc-dc converter and experimental verification of the converter efficiency in both forward and backward direction is also included. Chapter 6 presents the conclusion and recommendations for future work.

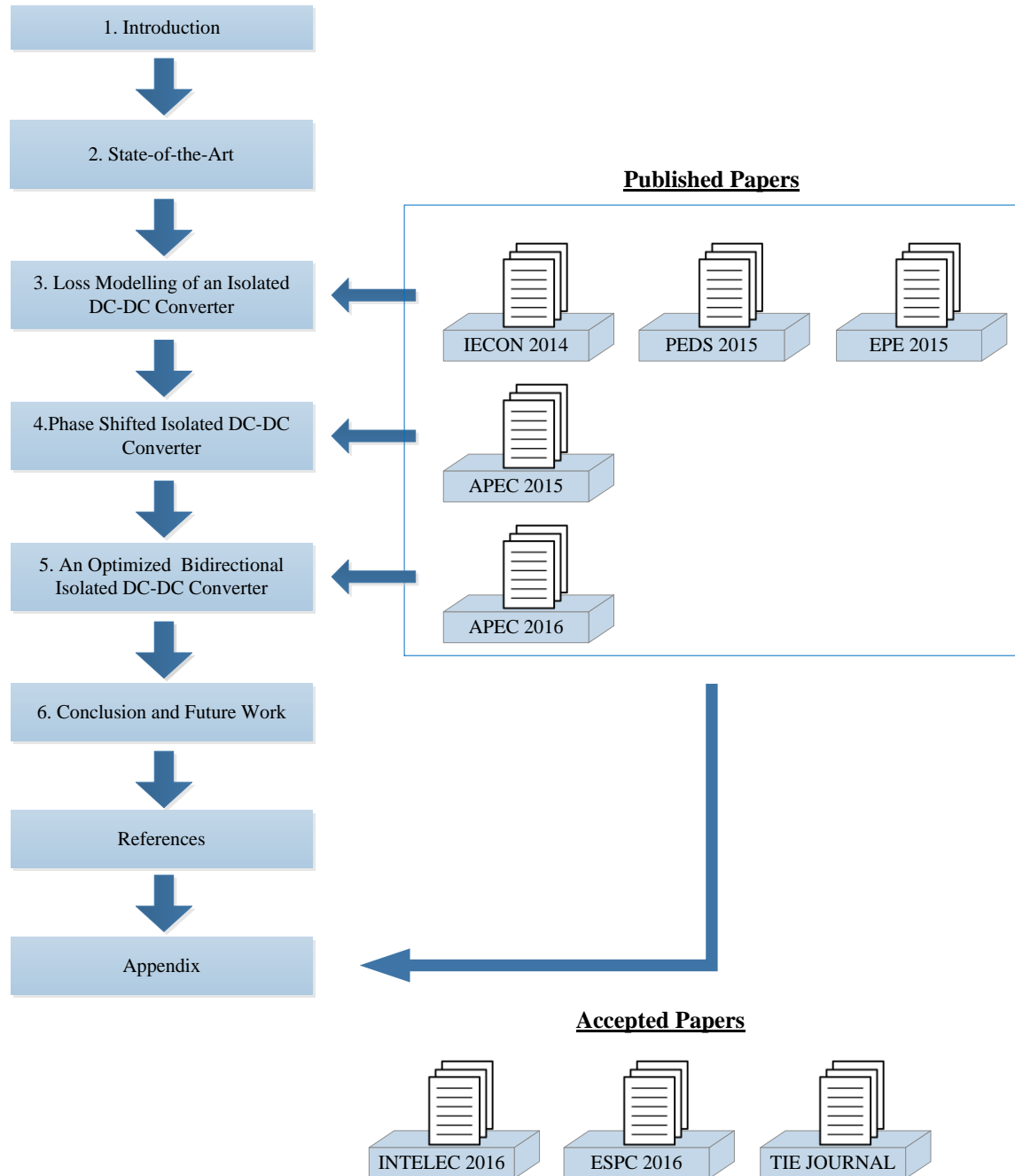


Fig. 1.2. Thesis structure

1.6. List of Publications

Different parts of the research outcomes presented in this thesis have already been published or will be published in various peer-reviewed international conferences and journals. The publications developed during this PhD work are:

- R. Ramachandran, M. Nymand, “Experimental Demonstration of a 98.8% Efficient Isolated DC-DC GaN Converter,” *IEEE Trans. Ind. Electron*, accepted for publication.
- R. Ramachandran, M. Nymand, N. H. Petersen, “Design of a compact, ultra-high efficient isolated DC-DC converter utilizing GaN devices,” in *Proc. of the Annual Conference of the IEEE Industrial Electronics Society, IECON 2014*, pp. 4256-4261, Oct/Nov 2014.
- R. Ramachandran, M. Nymand, “Design and Analysis of an Ultra-High Efficiency Phase Shifted Full Bridge GaN Converter,” in *Proc. of the Applied Power Electronics Conference and Exposition (APEC 2015)*, pp. 2011-2016, Mar 2015.
- R. Ramachandran, M. Nymand, “Analysis of capacitive losses in GaN devices for an isolated full bridge DC-DC converter,” in *Proc. of the International Conference on Power Electronics and Drive Systems (PEDS 2015)*, pp. 467-472, Jun 2015.
- R. Ramachandran, M. Nymand, “Switching losses in a 1.7 kW GaN based full-bridge DC-DC converter with synchronous rectification,” in *Proc. of the European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1-10, Sept 2015.
- R. Ramachandran, M. Nymand, “A 98.8% Efficient Bidirectional Full-Bridge Isolated DC-DC GaN Converter,” in *Proc. of the Applied Power Electronics Conference and Exposition (APEC 2016)*, pp. 609-614, Mar 2016.
- R. Ramachandran, M. Nymand, “An Energy Recovery Clamp Circuit for an Isolated DC-DC GaN Converter,” in *Proc. of the International Telecommunications Energy Conference (INTELEC 2016)*, accepted for publication.
- R. Ramachandran, M. Nymand, “Loss Modelling and Experimental Verification of a 98.8% Efficiency Bi-directional Isolated DC-DC Converter,” in *Proc. of the European Space Power Conference (ESPC 2016)*, accepted for publication.

2. State-of-the-Art

This chapter is divided into two sections. In the first section, a literature review on wide band gap devices and their advantages are presented along with a small discussion on some of the non-isolated dc-dc converters utilizing GaN devices. Later sections gives an overview of various high efficiency isolated dc-dc converters in the present state-of-the-art. This section also includes a literature review for bidirectional operation of various isolated dc-dc converters. Efficiency and power details of high efficiency isolated dc-dc converters in the literature are summarized and presented at the conclusion of this chapter.

Significant amount of scientific literature on high efficiency in isolated dc-dc converter has been reported in recent years, but comparing the efficiency of various converters is a major challenge. One of the challenges is the lack of reliable data on efficiency and measurement accuracy. Even though the power rating of the converter depends on specific applications, in order to have a fair comparison of various converters available in the literature, it is required to determine a ‘comparative’ power rating of the converter. A unified solution to determine the ‘comparative’ power rating of the converter is also discussed in this chapter.

In spite of lack of some of the data, this chapter presents an overview of published papers on various high efficiency isolated dc-dc converters and bidirectional isolated converters in the present state-of-the art.

2.1. Wide Band-gap Devices

Since 1960, Silicon has been used as a semiconductor material for power devices when Dawon Kahng at Bell laboratories invented the first MOSFET [1]. The material properties of Si in terms of energy gap, electric field, electron mobility and thermal conductivity may become a limiting factor in the near future. Advances in super junction technology in Si MOSFET will drag these limitations to a certain extent. However, the potential of wide band gap materials such as SiC and GaN will certainly make the world of power converters more compact and highly efficient. Table 2.1 shows the various material properties of Si, SiC and GaN as semiconductors for power devices [2].

Table 2.1: Material properties of Si, SiC and GaN

Material properties		Si	4H-SiC	GaN
Band-gap Energy (eV), E_g		1.12	3.2	3.4
Critical Electric Field Breakdown (MV/cm), E_{crit}		0.3	2.2	3.3
Intrinsic Concentration (cm^{-3}), n_i		1.4×10^{10}	8.2×10^{-9}	1.9×10^{-10}
Electron Mobility (cm^2/Vs), μ		1400	950	1500
Thermal conductivity (W/cm.K), λ		1.5	3.8	1.3

The material properties of these wide band-gap devices have a major influence on the fundamental performance characteristics. The wide band-gap of SiC and GaN results in very low intrinsic carrier concentration that gives negligible junction leakage current. This allows high temperature operation without excessive leakage or thermal runaway, if their packaging can withstand the temperature [2].

To optimize the power handling capability of a power device, the on-resistance of the device has to be minimized for a certain breakdown voltage. From [4], the on-resistance of the device is inversely proportional to the electron mobility and inversely proportional to the third power of energy gap of the semiconductor material.

$$R_{(ON)} \propto \frac{1}{\mu E_g^3} \quad (2.1)$$

Equation (2.1) shows that the semiconductor materials having high electron mobility and large energy gap has lower on-resistance and will have superior power handling capability. Theoretically, for a certain breakdown voltage, GaN devices can have 30 times lower on-resistance than their Si alternative and 2 times lower on-resistance than their SiC counterpart.

In order to increase the switching speed of the device, thereby reducing the switching losses, frequency response and trans-conductance have to be considered. Trans-conductance is directly proportional to electron mobility and square of energy gap. Frequency response of the device is proportional to the product of electron mobility and energy gap [4].

$$g_m \propto \mu E_g^2 \quad (2.2)$$

$$f_T \propto \mu E_g \quad (2.3)$$

Thus, due to the high band gap energy, GaN and SiC will have better frequency response and trans-conductance property compared to silicon.

From the above-mentioned material properties, we can conclude that GaN devices have superior material properties compared to Si, which will reduce the on-resistance and size of the device. Due to the improved frequency response, they are suitable for high frequency operation. High switching frequency reduces the size of the passive components used in the converter. Thus, a compact and highly efficient converter can be realized using GaN devices.

The only drawback of wide band gap device is the higher forward voltage drop. For a certain temperature and unit charge, the forward voltage in a pn-junction is directly proportional to the energy band gap, E_g . For the same current density, the forward voltage drop will be significantly higher in these wide band gap devices than in silicon.

GaN is a promising wide band gap semiconductor material for power converters in the near future. There are still some major challenges in the material manufacturability of GaN devices [5]. The cost of GaN material is two orders of magnitude costlier than silicon. GaN is not as mature technology as silicon nowadays. It is believed that in few years, GaN devices will have much more improvement and will reach a state where these devices will have cost equivalent to silicon [5].

Another major challenge in using these wide band gap devices is the packaging. These devices are suitable for high temperature and high frequency operation [5]. At high frequency operation, stray impedance of the entire circuit should be low [6]. Otherwise, the losses associated with switching increases and the advantages of GaN devices cannot be utilized to full extent [6], [8].

Some of the literatures available on non-isolated dc-dc converters utilizing GaN devices are discussed below:

A 180W boost converter with a switching frequency of 200 kHz is presented in [11], the maximum efficiency of the converter is 96.5%. Later, in [12], a 100W, 500 kHz boost converter utilizing GaN devices is presented. The maximum efficiency of the converter is 96%.

Boost converter utilizing GaN devices with a high switching frequency of 1MHz is reported recently in literature [13], [14]. In [13], a 300W, 175 to 350V boost converter is presented. The maximum efficiency of the converter is 98%. A 1.2 kW interleaved bidirectional buck/boost with and without a coupled inductor is presented in [14]. The efficiency comparison shows that the converter has a maximum efficiency of 98.5% with coupled inductor and 98.2% with a non-coupled inductor prototype. In [16], the design of a 2 kW, 540V to 270V buck converter for an aircraft application is presented for different switching frequencies and current ripples. The converter has exhibited a maximum power density of 7.4 kW/dm³ at a switching frequency of 24 kHz and a current ripple of 18A, while the maximum efficiency of 99.1% is achieved at a switching frequency of 65 kHz and 20A current ripple [16]. The paper [16] also concludes that high current ripple in a buck converter using WBG devices helps in reducing the transistor losses.

2.2. Isolated DC-DC Converter

Since there are only a few papers available on isolated dc-dc converters using GaN devices, it is worthwhile to have a literature review on isolated dc-dc converter with the highest conversion efficiency in the power range of 1-10 kW. In order to have a fair comparison of the efficiency, a unified solution to determine the ‘comparative’ power rating of the converter is discussed below:

Most of the power converters need to operate continuously over a wide range of load conditions, for e.g. 30 - 70% of output power, unless otherwise specified for special applications. Hence, a

converter designed for general applications should have higher efficiency during a wide range of load conditions. In order to assure high efficiency over this wide range, it is often preferable to have the peak efficiency of the converter around 50% of the full load. This will help in maintaining a flat efficiency curve over wide operating load conditions. This power rating of the converter, which will be almost twice the maximum efficiency power rating, is referred as the ‘comparative’ power rating in this thesis.

Various isolated dc-dc converters along with their topologies are considered for comparison of efficiency. For each published design, brief descriptions of the converter and the published efficiency results are also provided.

The Dual Active Bridge (DAB) is one of the common topologies in isolated dc-dc converters. The circuit diagram for a DAB isolated dc-dc converter is shown in Fig. 2.1.

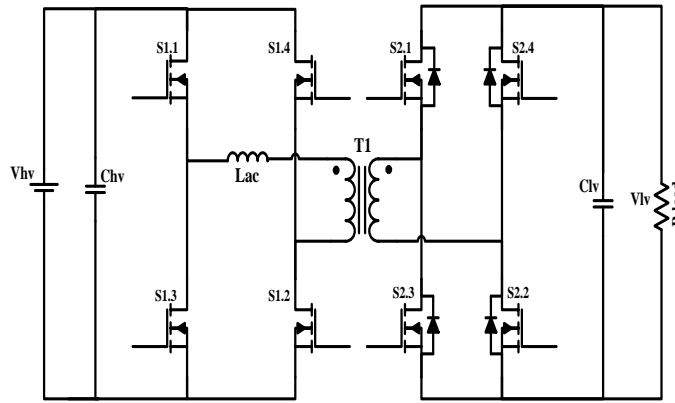


Fig. 2.1. Dual active bridge isolated dc-dc converter

In addition to the galvanic isolation, most DAB converters provide soft switching characteristics and bidirectional power flow [23]-[25]. However, in order to achieve high efficiency over a wide operating range, zero voltage switching over this entire power range and low circulating current are required. Various methods to improve the performance of DAB converters have been mentioned in the literature [26]-[28]. The ZVS range in DAB converter is limited by the voltage conversion ratio and the load conditions [26]. In order to increase the ZVS range, introduction of an external ac inductance or increasing the leakage inductance of the transformer is also proposed [28], [30].

In [17]-[18], a bidirectional isolated dc-dc converter for battery energy storage system is presented. The 6 kW DAB converter uses a transformer having a turns ratio of 6:1. IGBTs are used as the switching devices. In charging mode of operation, the converter is designed with an input voltage of 305-355V and a battery voltage of 50-59V at the output. At 20 kHz, the maximum efficiency of the converter is presented as 96% in charging mode and 96.9% in

discharging mode [17]. When the switching frequency is reduced to 4 kHz, the converter has achieved an efficiency of 98.1% in charging mode and 98.2% in discharging mode [18]. Since the highest efficiency of the converter occurs at 2.4 kW, in our comparison, the ‘comparative’ power rating of the converter can be considered as approximately 5 kW.

A 3.5 kW boost series resonant DAB bidirectional converter for an electric vehicle battery charger is presented in [29]. The converter presented has a nominal input voltage of 390V and battery voltage of 330V. Si super junctions (SJ) MOSFETs are used as the switching components. The switching frequency is varied from 120 kHz to 72 kHz depending on the output load. The efficiency curve of the converter at full load for various battery voltages is shown in the paper. The maximum efficiency of the converter is 97.5% at 330V of battery voltage.

Recently, a 3.3 kW bidirectional battery charger utilizing GaN devices for plug-in electric vehicle was reported in the literature [30], [31]. The switching frequency of the dual active bridge converter is 500 kHz. The efficiency of the converter with discrete inductor and transformer is compared with a converter equipped with an inductor and transformer integrated as one unit. The 250V input to 250V output converter has an efficiency of 97.2% at 1 kW with a discrete inductor and transformer. The efficiency of the converter with integrating inductor and transformer in a single unit has been increased to 98.2% [31]. Since, the efficiency of the converter is shown at 1 kW output power, the ‘comparative’ power rating can be considered as 2 kW.

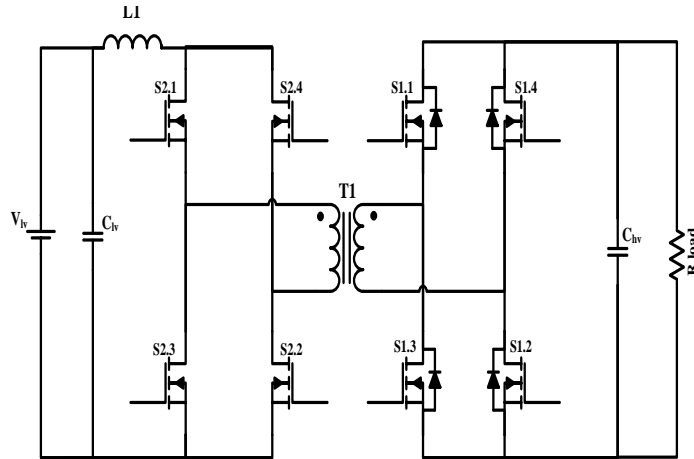


Fig. 2.2. Isolated full bridge boost converter

In [19], a hybrid LLC half-bridge resonant converter with phase-shifted PWM ZVZCS full-bridge converter is presented. The converter is rated for an output power of 6.6 kW. MOSFETs are used as switching devices in the lagging leg and IGBTs are used at the leading leg of the

converter. Efficiency curves are shown at a switching frequency of 91.5 kHz. The peak efficiency of the converter with 390V input and 390V output is 98.4%.

A 1.5 kW current-voltage fed dc-dc bidirectional converter is presented in [32]. The circuit diagram for an isolated boost converter is shown in Fig. 2.2. In boost mode, the input voltage of the converter is 28V and output voltage is 280V. The converter uses an active clamping branch and pulse width modulation control to reduce the switching losses in the devices. The highest efficiency of the converter is shown as 96% at an output power level of 750W and input voltage of 32V.

In [22], a 1.5 kW isolated boost converter with a voltage doubling circuit is presented. The paper has demonstrated the design of very low leakage inductance transformer and has achieved very high conversion efficiency. Low voltage power MOSFETs were used at the primary side of the converter and SiC rectifier diodes are used at the secondary side. Zero reverse recovery in SiC Schottky diodes also helps in improving the efficiency of the converter. The peak efficiency at the converter is 98%. The worst-case efficiency at maximum output power and minimum input voltage is 96.8%.

In [33], a 6 kW full bridge boost converter is presented. SiC MOSFETs are used as the switching devices at the low voltage side and IGBTs are used at the high voltage side. Planar magnetics are used for the design of the converter. The peak efficiency of the converter is 97.8% at a switching frequency of 40 kHz and input voltage of 80V. In buck mode of operation, the peak efficiency of the converter is 96.5%.

An on-board battery charger utilizing SiC power devices for electric vehicles is presented in [34]. The converter uses an isolated full-bridge buck topology as shown in Fig. 2.3. The peak efficiency of the isolated dc-dc converter is 96.5% at 200 kHz of switching frequency. The converter was designed for a switching frequency of 500 kHz, but the peak efficiency of the converter, with this switching frequency, has reduced to 93.9%.

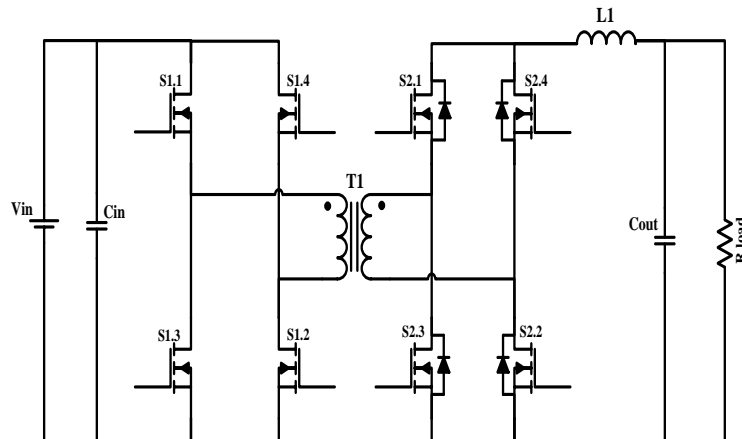


Fig. 2.3. Isolated full bridge buck converter

A 3 kW phase shifted full-bridge converter operating at a switching frequency of 200 kHz is presented in [35]. The peak efficiency of the converter is 96.8% at 50% of full load. The paper also shows how the efficiency drops with the increase in magnetizing current in a phase shifted converter.

In [36], a 5 kW, 400V to 54V phase shifted PWM converter for telecom applications is presented. The phase shift dc-dc converter is aimed to achieve an efficiency of 99%, but the maximum efficiency of the converter is shown as 98.5%. The converter utilizes a center tapped transformer and a split secondary rectifier. Split secondary uses twice the number of parallel switches compared to a two-winding transformer. The center tapped transformer increases the leakage inductance and has high dc resistance and dc winding current, which will reduce the efficiency of the transformer and hence the efficiency of the whole converter. The secondary side of the converter has used many devices in parallel, which reduces the efficiency of the converter, due to increased switching losses even though it reduces the conduction losses.

In [37], a 2 kW, 20 kHz bidirectional isolated converter for fuel cell electric vehicle with less device count is presented. The converter uses Si MOSFETs at low voltage side and IGBTs at high voltage side. Even though the active device count reduces from a conventional full bridge bidirectional converter, the number of inductors and capacitors used in the converter has increased. In buck mode of operation, the efficiency of the converter is 96% at 1200W of output power and in boost mode; the converter has an efficiency of 96% at 600W output power.

In [38], a buck/boost derived bidirectional isolated topology with an output power of 5 kW and a switching frequency of 20 kHz is presented. Soft switching and soft-start capability of the converter is also discussed in the paper. The converter has shown a maximum efficiency of around 95% in both buck and boost mode of operation.

2.3. Summary

From the material properties of GaN, it is advantageous to use such materials in power devices to make the converters more compact in size and highly efficient. Researches on SiC devices in high power converters are discussed in various papers but use of GaN devices mainly in isolated dc-dc converter is rarely found in the literature. Moreover, we can conclude from literature that compared to SiC, GaN devices will be advantageous in few kW applications where the voltage rating of the transistors is up to 1 kV [4], [5]. Even though significant amount of researches in GaN devices on material properties and in low power high frequency applications are discussed and published, the application of these devices in high power converters are scarcely available.

A short summary of various high efficiency isolated dc-dc converters is given in Table 2.2. Except [22], all the converters in the literature use soft switching topologies and the efficiencies are measured at high input voltage and maximum switch duty cycle.

Ultra-high Efficiency DC-DC Converter using GaN Devices

In Table 2.3, a summary of various bidirectional isolated dc-dc converters and their efficiency details are presented.

Table 2.2: State-of-the-art comparison of various high efficiency isolated dc-dc converters

No	Topology	Power Level ^[1] (W)	Comp. Power ^[2] (W)	Semiconductors Used		Switch Freq. (kHz)	Efficiency		Ref.
				Pri.	Sec.		Max. (%)	Power (W)	
1	DAB	6000	4200	IGBT	IGBT	20	96.9	2100	[17]
2		6000	4800	IGBT	IGBT	4	98.1	2400	[18]
3		3300	2000	GaN	GaN	500	98.2	1000	[31]
4	Resonant	6600	7000	Si	Si	91.5	98.4	3500	[19]
5		1000	1200	Si	Si	100	97.5	600	[21]
6	Isolated Boost	1500	2000	Si	SiC	45	98	1000	[22]
7		1500	1500	Si	Si	100	96	750	[32]
8		6000	6000	SiC	IGBT	40	97.8	3000	[33]
9	Isolated Buck	6100	8000	SiC	SiC	200	96.5	4000	[34]
10		3000	3000	Si	Si	200	96.8	1500	[35]
11		5000	5000	Si	Si	25	98.5	2500	[36]

Table 2.3: State-of-the-art comparison of various bidirectional isolated dc-dc converters

No	Topology	Power Level ^[1] (W)	Switch Freq. (kHz)	Forward operation Efficiency		Backward operation Efficiency		Ref.
				Max. (%)	Power (W)	Max. (%)	Power (W)	
1	DAB	6000	20	96.1	2400	96.9	2100	[17]
2		6000	4	98.1	2400	98.2	1300	[18]
3		3000	20	97.1	1000	96.7	1500	[39]
4	Resonant	1000	100	97	600	97.5	600	[21]
5		1000	100	95.7	850	96.1	850	[40]
6	Isolated Buck/Boost	6000	40	96.5	3000	97.8	3000	[33]
7		2000	20	96	1200	96	600	[37]
8		5000	20	94.8	1750	95	800	[38]

^[1]Power rating mentioned in the respective published paper

^[2] ‘Comparative’ power rating of the converter, which is twice the maximum efficiency power rating

Soft switching in an isolated dc-dc converter has been used mainly to reduce the output capacitive losses in the switching devices; this is mostly realized at the expense of reducing efficiency of the transformer or introducing an external inductance. Nowadays, as the switching

devices are getting more and more ideal, output charge of the devices reduces and thus, the capacitive switching losses for a certain frequency is smaller. If the efficiency of the magnetics can be improved, then soft switching may not be required to achieve ultra-high efficiency in isolated dc-dc converters.

From all the above discussion of various high efficiency isolated dc-dc converter, it is highly desirable to have a bidirectional converter, which has high efficiency in both directions with a flat efficiency curve at a considerably higher switching frequency than the present state-of-the-art. The design and analysis of such an isolated dc-dc converter utilizing GaN devices in the power range of 1 to 2.5 kW will be discussed in the next chapters.

3. Loss Modelling of an Isolated DC-DC Converter

In order to further improve the efficiency of an isolated dc-dc converter above the present state-of-the-art, it is necessary to have a clear understanding of various power losses in the converter. This chapter will focus on the analytical loss modelling of an isolated dc-dc converter. The chapter starts with the operation principle of an isolated dc-dc buck converter followed by a comprehensive analytical loss modelling for the converter. Further, in this chapter, experimental results from a 1.7 kW isolated dc-dc buck converter are also presented.

Design and implementation of a 1.7 kW GaN converter with experimental results is also published as a conference paper [A1].

3.1. Operation of an Isolated DC-DC Buck Converter

The schematic diagram of an isolated dc-dc buck converter is presented in Fig. 3.1. The timing diagram with basic operational waveforms is presented in Fig. 3.2.

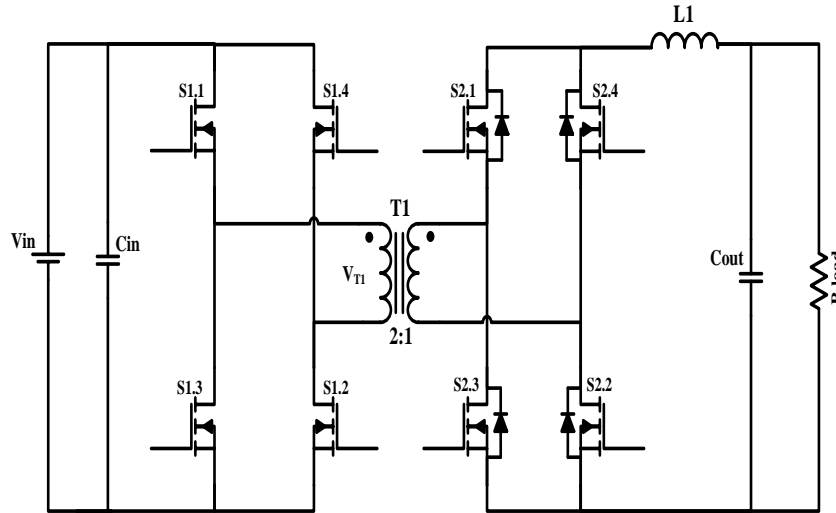


Fig. 3.1. Schematic diagram of an isolated full bridge buck converter

Primary switches S1.1 and S1.2 are driven by the same PWM signal. Switches S1.3 and S1.4 are also driven by the same PWM signals but complement to S1.1 and S1.2 signals. Primary switches S1.1 – S1.4 are hard switched. The duty cycle D of each switch should be less than 50% to avoid cross conduction of the primary switches.

The operation of the isolated dc-dc full bridge buck converter is shown in Fig. 3.3 - Fig. 3.6 and is explained as follows.

A. Time interval between T_0 - T_1 (Fig. 3.3)

During this time interval, primary switches S1.1 and S1.2 are conducting. The reflected load current at the primary side flows through the switches S1.1 and S1.2. At the secondary side of the transformer, switches S2.1 and S2.2 are conducting and the inductor L1 is charging with a slope $\frac{(V_{in}/n - V_o)}{L_1}$, where V_{in} is the input voltage and V_o is the output voltage. The energy transfer from the input to the output occurs during this interval, so interval T_0 - T_1 is called the power transfer stage. This period ends when the primary switches S1.1 and S1.2 are turned off.

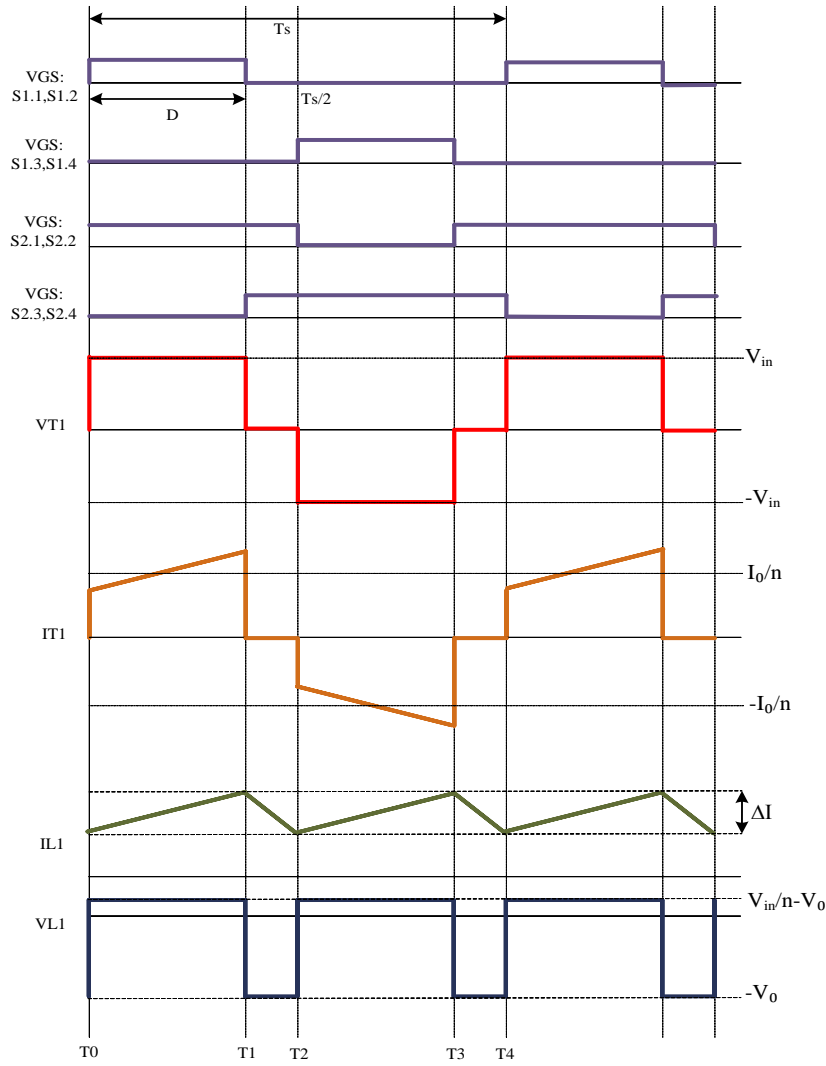


Fig. 3.2. Timing diagram and operational waveforms of an isolated buck converter

B. Time interval between T_1 - T_2 (Fig. 3.4)

All the switches in the primary side of the converter are turned off and all the secondary switches are conducting. The inductor current starts to freewheel in the secondary switches.

During this interval, there will be no energy transfer between the input and the output load. This stage is called the freewheeling stage.

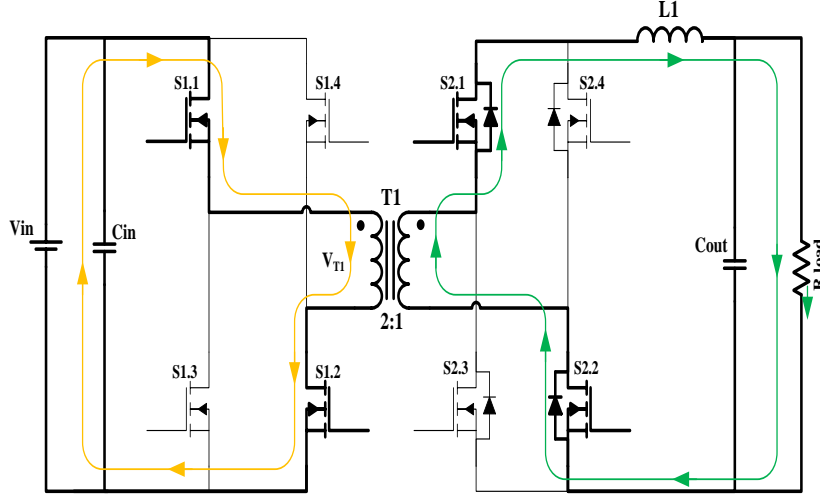


Fig. 3.3. Isolated buck converter operation: time interval between T0-T1

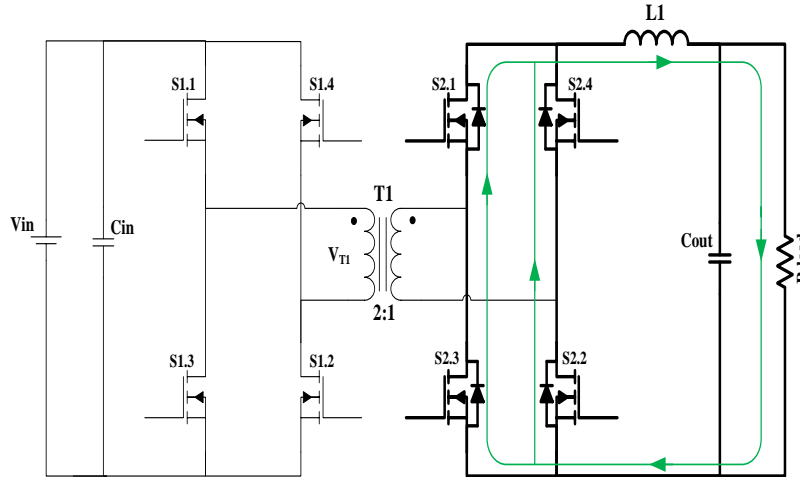


Fig. 3.4. Isolated buck converter operation: time interval between T1-T2

C. Time interval between T2-T3 (Fig. 3.5)

This period starts when the secondary switches S2.1 and S2.2 are turned off and primary switches S1.3 and S1.4 are turned on. Reflected inductor current flows from the input capacitor, C_{in} through switch S1.4, transformer T1, switch S2.4, inductor, L1 to the output and the current returns through the switches S2.3 and S1.3 to the input. This stage is also a power transfer stage.

D. Time interval between T3-T4 (Fig. 3.6)

Primary switches S1.3 and S1.4 are turned off and the secondary switches S2.1 and S2.2 are turned on. The secondary winding of the transformer is virtually shorted and the inductor current starts to discharge. This interval is similar to the time interval between T1-T2. This stage is also called the freewheeling stage.

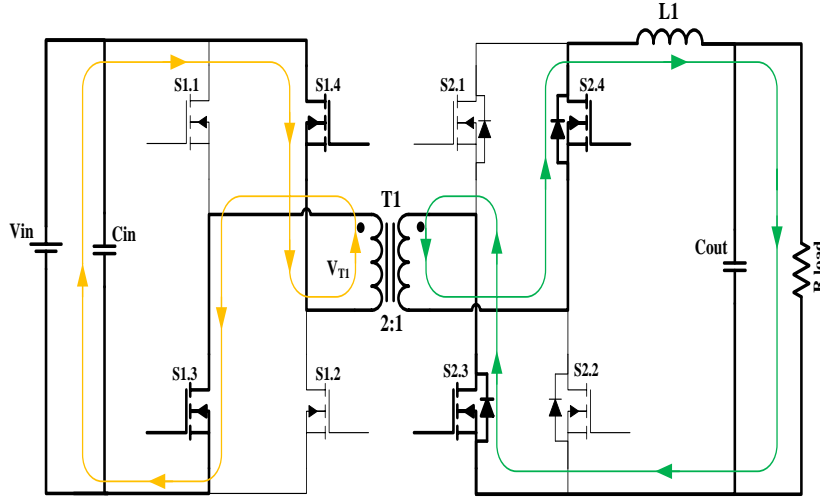


Fig. 3.5. Isolated buck converter operation: time interval between T2-T3

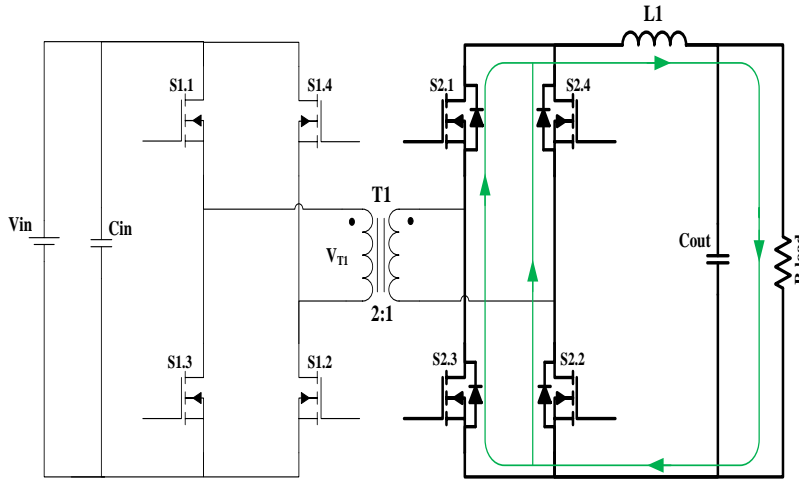


Fig. 3.6. Isolated buck converter operation: time interval between T3-T4

The output voltage of the isolated forward converter is given by:

$$V_o = \frac{2}{n} D V_{in} \quad (3.1)$$

where n is the transformer turns ratio (No. of primary turns/No. of secondary turns) and D is the duty cycle of the switch.

Switching frequency of inductor, f_L is twice the switching frequency of the switches, f_{sw} .

$$f_L = 2f_{sw} \quad (3.2)$$

3.2. Selection of Switching Frequency

Achieving the highest possible conversion efficiency in an isolated dc-dc converter is the major objective of this research project. Therefore, to select the optimum switching frequency, the efficiency of the converter at full load and half load conditions as well as the power density of the magnetics at various switching frequency are estimated and plotted in Fig. 3.7.

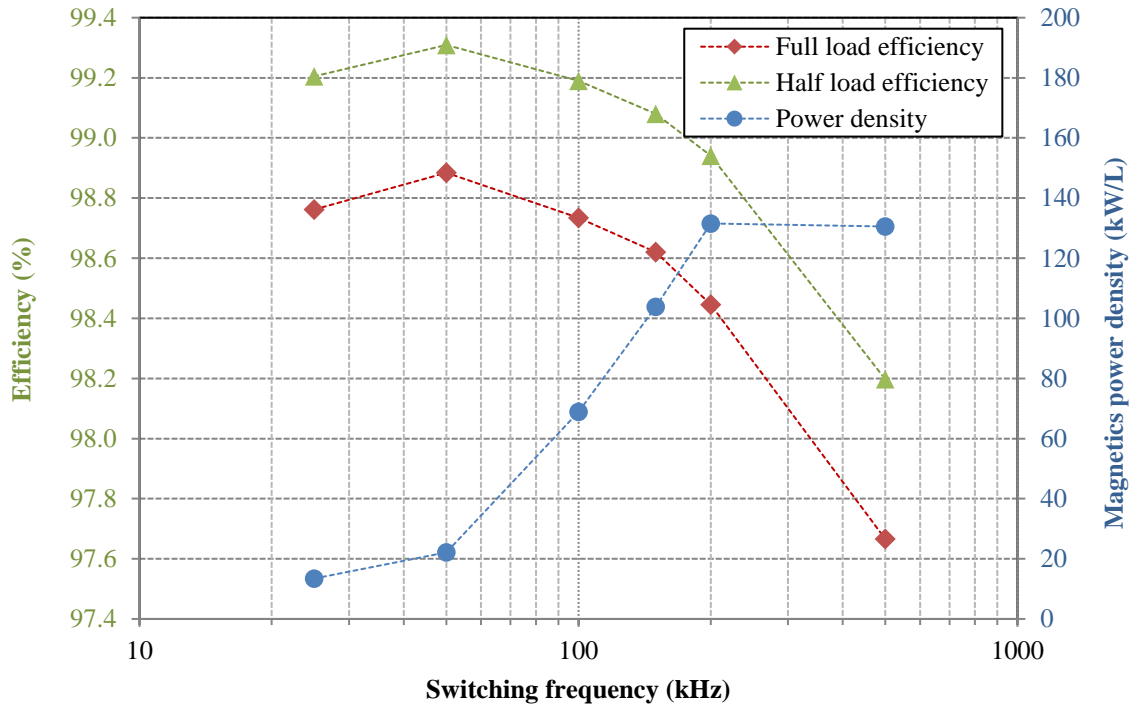


Fig. 3.7. Efficiency and power density of magnetics at various switching frequency

Even without considering the ac-resistance loss and the high frequency losses in magnetics, the converter efficiency reduces after 50 kHz. From Fig. 3.7, the power density of the magnetics increases with increase in switching frequency, but the size of the heat sink also increases due to the increase in power loss at higher switching frequency. This will further reduce the size of the whole converter and reduces the converter power density at higher switching frequency. Considering factors such as penetration depth, copper fill-factor, circuit parasitic, etc. and to

realize a very high efficiency magnetics, the switching frequency of the converter has been selected as 50 kHz.

3.3. Loss Modeling for Individual Power Components

In any power converters, the elements (capacitors, inductors and power semiconductors) used are non-ideal in nature. Therefore, there will be a voltage drop when a current flows through them and this causes power dissipation. In order to understand and improve the efficiency of individual elements, a loss modelling of major components in an isolated dc-dc converter has to be carried out. The major components constitutes transformer, inductor, switching devices and filter capacitors.

The power losses in a converter can be allocated into three major losses-idle loss, loss due to diode voltage drop and resistive loss. Idle losses are constant losses and they are almost independent of the output load current. Diode voltage drop depends directly on the output current and resistive losses are dependent on the square of the output current. In other words, the losses in a power converter can be expressed by a second order quadratic equation as a function of output current. Thus, the total power loss in a converter can be given by the equation

$$P_{tot} = k_o + k_1 I_o + k_2 I_o^2 \quad (3.3)$$

where, k_o is the idle losses which includes the core loss in magnetics, device drive losses and capacitive losses, k_1 is the loss factor associated with the diode voltage drop in the converter and k_2 is the loss factor associated with the resistive losses in the converter. The capacitive loss mentioned in the idle loss includes capacitive losses from the magnetics as well as the output capacitive switching losses from the power semiconductor devices. It is a constant value for a certain switching frequency and input voltage.

The design considerations of individual power components along with their loss modeling for an isolated dc-dc buck converter are discussed below:

3.3.1. Transformer

3.3.1.1. Design Considerations

The high frequency transformer provides galvanic isolation between the source and the load. In order to design an ultra-high efficiency transformer, selection of proper core material and windings are crucial. Ferrite materials have been a proper choice for high frequency transformer for many decades due to their high electrical resistivity and low eddy current losses [41]. Since, Ferroxcube 3C95 shows a flat power loss density variation with temperature, they were selected as the core material [42]. Traditional ferrite materials shows low losses at 100°C,

but the designed transformer is expected to work at a core temperature of less than 50°C, which makes 3C95 material a better choice among various other ferrites.

The selection of transformer winding is highly dependent on switching frequency. Copper foils are good choice if the operating frequency is less than 200 kHz; this is due to their large cross-sectional area with a minimum conductor thickness. This reduces the dc-resistance in the transformer winding and hence the losses. Above 200 kHz of operating frequency, Litz wires may be a good option, since at this high frequency, skin depth is very small and insulation thickness exceeds the copper area in copper foil windings. Therefore, at a higher frequency, when the copper foil with appropriate foil thickness will become impractical, Litz wire windings can be used. The optimum selection of number of strands in the Litz wire, to have lower losses will be another challenging factor for designing such transformers.

The main challenge in the design of a high frequency power transformer with high current rating is the reduction of ac-resistance in the transformer windings. Extensive interleaving of primary and secondary winding reduces the proximity effect and hence dramatically reduces the ac-resistance of the transformer [22].

The ac-resistance factor, F_R of a transformer winding is expressed as the ratio of ac-resistance, R_{ac} to dc-resistance, R_{dc} . F_R for a multi-layer transformer winding ($m > 1$) can be calculated from the equation [22],

$$F_R = \frac{R_{ac}}{R_{dc}} = \varphi \frac{\sinh 2\varphi + \sin 2\varphi}{\cosh 2\varphi - \cos 2\varphi} + \frac{2(m^2-1)}{3} \varphi \frac{\sinh \varphi - \sin \varphi}{\cosh \varphi + \cos \varphi} \quad (3.4)$$

where, $\varphi = h/\delta$

Since the winding thickness and the number of turns are different for primary and secondary windings, the ac-resistance factor will be also different. The effective ac-resistance factor, F_{RT} is calculated as the average of primary, F_{RP} and secondary winding resistance factors, F_{RS} .

$$F_{RT} = \frac{F_{RP} + F_{RS}}{2} \quad (3.5)$$

Another challenge in the transformer design is the reduction of leakage inductance. Leakage inductance of the transformer referred to primary is dependent on the primary turns and the primary-secondary winding intersections. By providing a few turns and extensive interleaving of primary and secondary winding, the leakage inductance will reduce drastically.

Leakage inductance in a transformer can be expressed by the equation [58],

$$L_{LK} = \mu_0 \frac{N^2 l_w}{M^2 b_w} \left[\frac{1}{3} \sum h p + \sum h \Delta \right] \quad (3.6)$$

From the above equation, leakage inductance is inversely proportional to the square of M , number of primary–secondary intersections. Hence, it is clear that extensive interleaving of primary and secondary winding will dramatically reduce the transformer leakage inductance and thereby reduces the energy stored in the leakage inductance.

3.3.1.2. Loss Modeling

The losses in a transformer constitutes of both core loss and copper loss. The core loss per unit volume for the transformer core can be calculated by the Steinmetz equation [43], given as

$$P_v = k f^\alpha \hat{B}^\beta \quad (3.7)$$

where, k , α , and β are the Steinmetz parameters of the ferrite material. In most cases, the parameters can be extracted from the core datasheet, in which they often provide core losses per unit volume as a function of frequency, flux density and temperature.

The main drawback of Steinmetz equation is that it is only valid for sinusoidal voltage excitation. Transformers used in an isolated dc-dc converter are subjected to non-sinusoidal excitations. The core loss can be higher than the calculated value even when the peak magnetic flux density and the switching frequency remains the same [44], [45]. Improved Generalized Steinmetz Equation (IGSE) can be used to overcome this limitation [45].

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB(t)}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt \quad (3.8)$$

where, $k_i = \frac{K}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta}$

By using IGSE and Steinmetz parameters as mentioned in (3.7), core loss for any flux excitation can be calculated.

The second source of loss in a transformer is the copper loss, which can be calculated from the resistance of the transformer winding and the RMS current flowing through them. In order to accurately find the copper loss in a transformer, the ac-resistance has been measured.

The transformer is designed with a specification given in Table 3.1. The penetration depth in copper is 0.29mm at 50 kHz. In order to reduce the ac resistance in the transformer, copper foils of 0.2mm and 0.4mm width are selected for the primary and secondary windings, respectively. Considering all the required clearances, the proposed core can accommodate 6 turns at the primary side and 12 turns at the secondary. The width of copper foil is selected as 25mm. The winding configuration of the transformer is shown in Fig. 3.8.

Table 3.1: Transformer specification

Power rating	P_o	1.7 kW
Input voltage	V_{in}	130 V
Transformer turns ratio	$n:1$	2:1
Switching frequency	f_{sw}	50 kHz
No. of turns in the primary winding	N_p	12 turns
No. of turns in the secondary winding	N_s	6 turns
Transformer core		EE55/28

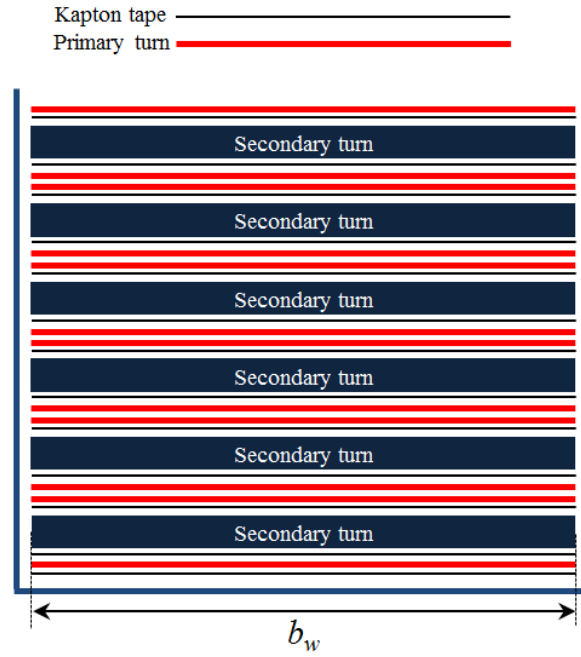


Fig. 3.8. Transformer winding configuration

Table 3.2: Transformer calculated and measured values referred to high voltage side

Transformer Parameters		Calculated	Measured
Magnetizing Inductance	L_m	1.42mH	1.437mH
Leakage Inductance	L_{lk}	24.11nH	37.05nH
Percentage of leakage to magnetizing inductance	L_{lk}/L_m	0.0017%	0.0026%
Resistance Factor	F_R	1.013	1.039
ac resistance	R_{ac}	11.50mΩ	11.83mΩ
dc resistance	R_{dc}	11.35mΩ	11.39mΩ

The ac-resistance and leakage inductance of the proposed transformer has been calculated using (3.4) and (3.6) respectively. Keysight 4294A precision impedance analyzer is used to validate the calculated parameters of the transformer and the measurement results are shown in Fig. 3.9. The calculated and the measured transformer parameters are presented in Table 3.2. The small variation in the leakage inductance is due to not considering the termination of transformer windings and the air space between primary and secondary windings in calculation.

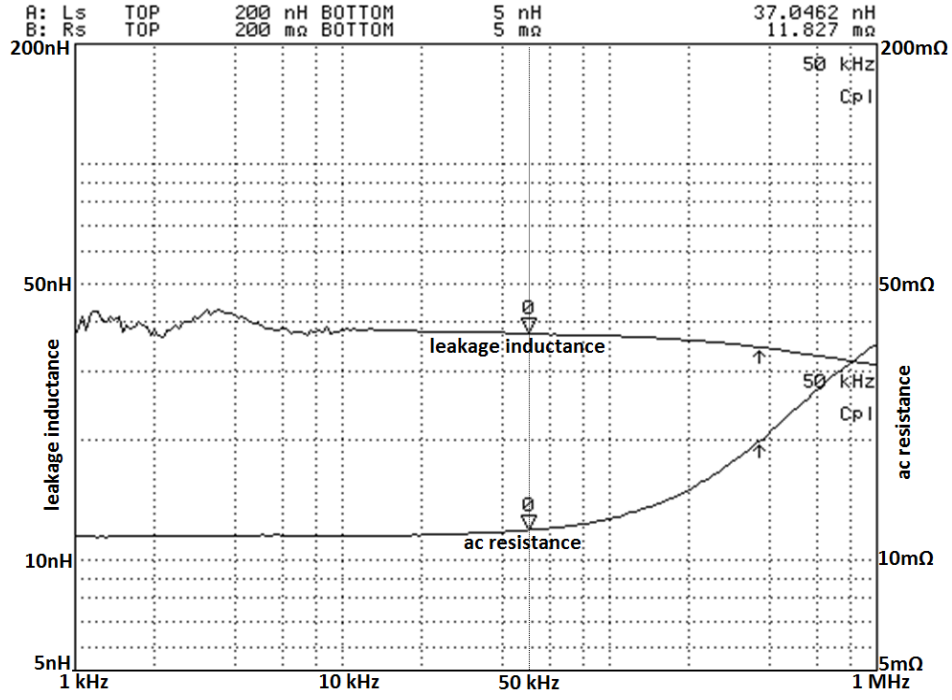


Fig. 3.9. Measured leakage inductance and ac resistance of the transformer referred to high voltage side

The current flowing through the transformer in an isolated dc-dc buck converter is shown in Fig. 3.10.

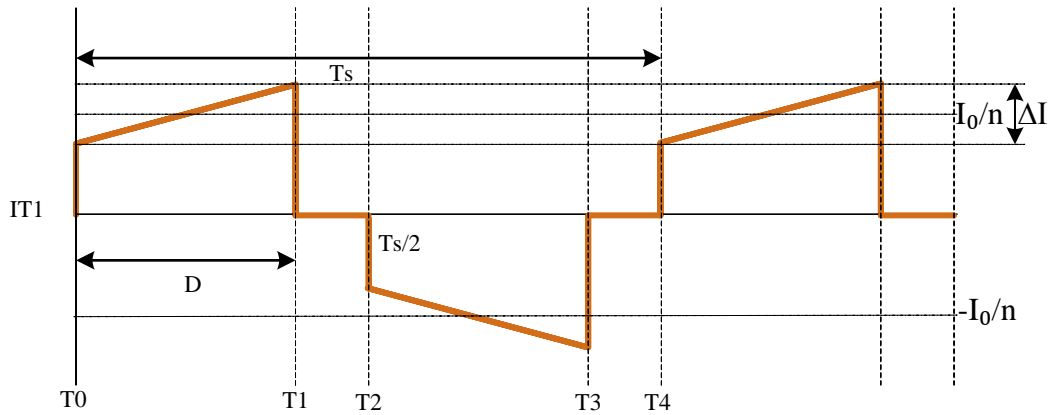


Fig. 3.10. Transformer primary winding current waveform for an isolated buck converter

The RMS current in the transformer winding can be calculated by the equation given below

$$I_{RMS,tfr} = \frac{I_o}{n} \sqrt{2D \left[1 + \frac{1}{12} \left(\frac{n \Delta I}{I_o} \right)^2 \right]} \quad (3.9)$$

Therefore, the copper loss in the proposed transformer can be calculated by

$$P_{Cu,tfr} = R_{ac} I_{RMS,tfr}^2 \quad (3.10)$$

The power loss equation for the transformer can be expressed as a function of output load current, I_o

$$P_{tfr} = k_{tfr,o} + k_{tfr,2} I_o^2 \quad (3.11)$$

$$k_{tfr,o} = k_{cap} + P_v V_e \quad (3.12)$$

where, k_{cap} represents the capacitive losses in the transformer winding

$$k_{tfr,2} = \frac{P_{Cu,tfr}}{I_o^2} \quad (3.13)$$

3.3.2. Inductor

3.3.2.1. Design Considerations

For an isolated dc-dc buck converter, minimum inductance, L_{min} required can be derived from the inductor current and the voltage waveform as shown in Fig. 3.11.

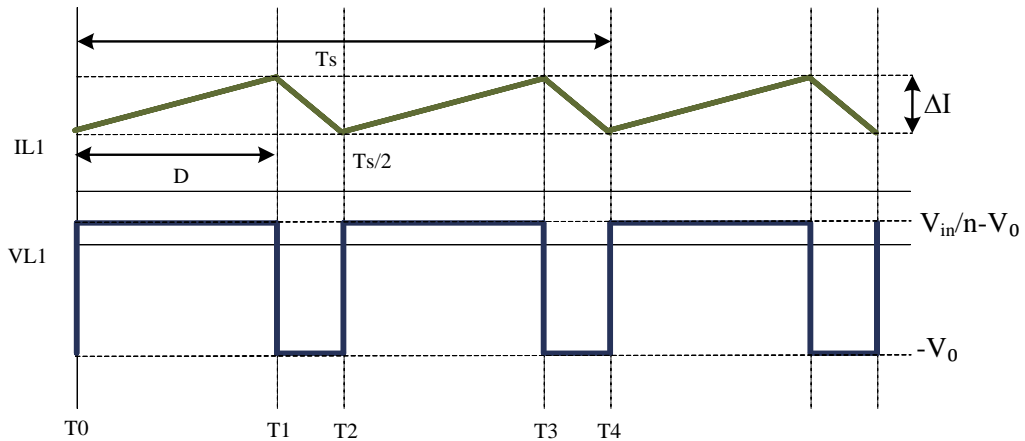


Fig. 3.11. Inductor current and voltage waveform in an isolated dc-dc buck converter

The relation between the voltage across the inductor, v_L and current through the inductor, I_L can be expressed by the basic equation:

$$v_L = -L \frac{dI_L}{dt} \quad (3.14)$$

During the interval T0 to T1, the voltage across the inductor is given by

$$v_L = \frac{V_{in}}{n} - V_o \quad (3.15)$$

Hence, the minimum value of inductance, L_{min} can be given by the equation

$$L_{min} = \frac{(\frac{V_{in}}{n} - V_o)}{\Delta I} D_L T_L \quad (3.16)$$

$$D_L = 2D \quad (3.17)$$

Proper selection of core material and the windings plays a crucial role in increasing the efficiency of the inductor and thereby increasing the conversion efficiency of the whole converter.

The inductors used in an isolated dc-dc converter operate under a high dc-bias current with a comparatively smaller ac ripple. Kool Mu powder cores are highly recommended in such applications. These materials have low core loss per unit volume and relatively high saturation level. Fringing losses are completely absent in these cores due to distributed airgaps in the material. Compared to ferrite materials, powder core materials exhibit soft saturation, which will allows safe operation without any inductance collapse at much higher currents [47].

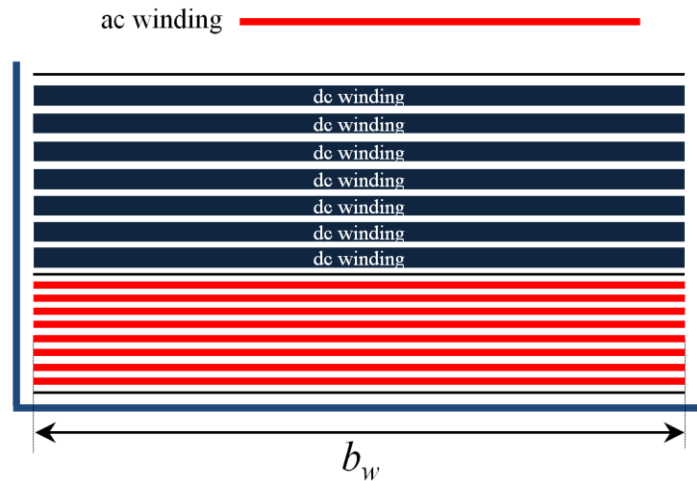


Fig. 3.12. Inductor winding configuration

Copper foil windings are preferred in high dc bias current applications since they have low dc-resistance. As the thickness of the copper foil increases, the ac-resistance of the winding also increases. In order to reduce the ac-resistance of the inductor winding, a two winding technique is used to design the inductor. Detailed explanation of two winding inductor design is explained in [48]. The winding configuration of the inductor with both ac and dc windings is shown in Fig. 3.12.

3.3.2.2. Loss Modeling

Similar to transformer loss modelling, inductor losses can be also modelled as a function of output current by a second order quadratic equation.

$$P_{ldr} = k_{ldr,o} + k_{ldr,2}I_o^2 \quad (3.18)$$

where, $k_{ldr,o}$ includes the idle losses in the inductor which constitutes the core loss and the capacitive losses from the inductor windings. $k_{ldr,2}$ corresponds to the copper losses associated with the inductor windings.

As explained in the inductor design, two windings are used for the inductor; a thin ac winding and a thick dc winding. The low impedance ac winding was placed inner most close to the center leg of the core and mostly carries the ac ripple current. The dc winding are placed outside the ac winding and mainly carries dc due to their low dc resistance. The ac and the dc windings are interconnected at the winding terminals.

The dc winding losses in a two winding inductor is same as a single winding inductor but the ac winding losses reduces tremendously. The dc winding loss in an inductor can be given by

$$P_{W,dc} = \frac{\rho_c l_w}{A} I_{dc}^2 \quad (3.19)$$

The ac resistance of the ac winding is comparatively smaller than the dc winding. So, assuming $\frac{2}{3}$ of the ac current flows through the thin ac winding and the remaining $\frac{1}{3}$ flows through the thick dc winding. The ac winding loss in the two windings, for a triangular inductor current can be calculated as [48]

$$P_{W,ac} = R_w^* \left[\frac{K_{r,dc}}{4} + K_{r,ac} \right] \left[\frac{\Delta I}{3\sqrt{3}} \right]^2 \quad (3.20)$$

where, R_w^* is the dc resistance of the winding with a thickness of one penetration depth, $K_{r,dc}$ and $K_{r,ac}$ are the normalized effective resistance factor.

Therefore, the total copper loss in the two-winding inductor can be given by,

$$P_{Cu,ldr} = P_{W,dc} + P_{W,ac} \quad (3.21)$$

3.3.3. Power Semiconductor Devices

3.3.3.1. Design Considerations

GaN devices are selected as the power semiconductor devices for the isolated dc-dc converter. Some of the advantages of GaN FETs compared to a Si MOSFET are discussed below:

Due to the lateral structure of GaN FET, they have a very small gate to drain capacitance, C_{GD} compared to vertical Si MOSFETs. GaN FETs shows good dv/dt immunity since they have a slightly larger gate to source capacitance, C_{GS} than C_{GD} . This helps in reducing the delay time at the switching instant of GaN FETs [49].

Optimum design of the drive circuit is one of the major challenges of using GaN FETs in high power converters. They have a very low gate threshold voltage. The GaN FETs from Efficient Power Conversion (EPC) have a gate threshold voltage of 1.6V [50]. Care must be taken to ensure low impedance path from gate to source to avoid the device to turn-on and turn-off inadvertently.

GaN devices have low maximum gate drive voltage compared to Si MOSFET. This also reduces the gate drive loss since the loss is directly proportional to the gate drive voltage. The maximum gate voltage that can be applied to an EPC GaN FET is only 6V. The major concern with the low gate voltage of GaN FET is the high side or floating side supply in half bridge configuration. LM5113, LM5114, UCC27611, UCC27511 from Texas Instruments are high-speed gate drivers optimized for e-mode GaN FETs.

The switching speed of FET is affected by the parasitic inductance of the gate drive circuit. Loop inductance in the drive circuit can be reduced by placing the driver as close as possible with the GaN FETs. The gate traces, both positive and negative are advisable to run parallel to each other. An LCR resonant circuit is formed between the parasitic inductance, gate capacitor and the driver pull down path. This will cause ringing at the gate of the FET. An optimum resistor can be introduced in the LCR circuit to damp the gate oscillations.

Proper PCB layout is required for the reliable operation of GaN FETs [51]. In order to reduce the switching losses of the device, the turn-on and turn-off should be as fast as possible. The gate drive should provide the required peak current to achieve the switching speed. This is determined by the dv/dt rating of the GaN FET.

LM5114 is able to drive multiple GaN FETs in parallel due to their strong sink current capability. The inputs for these driver ICs are TTL/CMOS logic. They are suitable for high frequency operation due to their fast switching speed and minimized propagation delay [52].

One of the challenges in fast switching of power devices in a half bridge configuration is “Miller effect”. This is more prominent when driving the device without a negative voltage. When the high side switch is turned on, a voltage change, dv/dt occurs at the low side switch. This voltage change will allow a current to flow through the gate drain capacitance, gate resistor and the driver resistor. This creates a voltage drop across the gate resistor. If this voltage exceeds the threshold voltage of the low side switch, then it turns on the device unintentionally.

Introducing separate gate turn-on and turn-off resistor is one of the solutions to this problem. Accidental turn-off of the switch can be avoided by reducing the turn-off resistor. But this may increase the ringing at turn off due to the parasitic inductance. So optimized value of turn-on and turn-off resistors are necessary to have a trade-off between the gate voltage overshoot and gate ringing. Gate driver LM5114 is a good choice since it has a split output for both turn-on and turn-off resistors.

The ‘body diode’ characteristic is another major feature of GaN FETs. Like conventional Si MOSFET, GaN devices also show a reverse conduction mechanism. Due to purely lateral structure of GaN devices, they do not have a parasitic bipolar junction. That is the reverse conduction mechanism is not similar to conventional MOSFETs. With zero bias on the gate and the drain-voltage is decreased, electrons are injected into the gate creating a positive bias across the gate. Once the gate threshold voltage is reached, the electron under the gate form a conduction channel and the device starts conducting in reverse direction [50]. The major advantage of using GaN FETs in reverse conduction is that, there is no minority carrier involved in this conduction, so there will not be any reverse recovery losses. This is highly advantageous in synchronous rectification applications.

In reverse conduction, the forward voltage drop of GaN FET is higher compared to Si MOSFET body diode. Hence, the dead time should be optimized to reduce the reverse conduction period. This helps in improving the efficiency of the converter. Due to the fast switching characteristics of GaN FETs, dead time in GaN converters can be reduced tremendously compared to conventional Si converters [54].

3.3.3.2. Paralleling of GaN FETs

In order to increase the power rating of the converter, and to reduce the conduction losses from the power semiconductor devices, paralleling is the best option. GaN FETs shares many similarities with conventional Si MOSFET regarding paralleling of devices. GaN FETs exhibit positive temperature coefficient for on-resistance, which facilitates the parallel operation.

To find out more about the advantages of paralleling GaN FETs, device capacitances of the EPC2010 are compared with some commercially available 200V Si MOSFET and is shown in Table 3.3.

Table 3.3: Comparison of device capacitance between GaN FET and Si MOSFET

Parameters	EPC2010	Si MOSFET #1	Si MOSFET #2	Si MOSFET #3
$R_{DS(ON)} \text{ (m}\Omega\text{)}$	18m Ω	23m Ω	17m Ω	11.7m Ω
$C_{iss} \text{ (pF)}$	480	4800	5200	5000
$C_{oss} \text{ (pF)}$	270	300	350	400
$C_{rss} \text{ (pF)}$	9.2	100	80	6

As the devices are paralleled the resistive losses associated with the on-resistance is reduced but the idle losses, both capacitive switching loss and gate drive losses increase.

The output charge, Q_{oss} can be calculated from output capacitance, C_{oss} vs voltage and can be defined as

$$Q_{oss} = \int_0^V C_{oss}(v) dv \quad (3.22)$$

Drive loss can be calculated from the maximum drive voltage, V_d and the switching frequency, f_{sw}

$$P_{drive} = V_d Q_G f_{sw} \quad (3.23)$$

Table 3.4: Comparison of Si MOSFET with GaN FET for a normalized on-resistance

Parameters	EPC2010	Si MOSFET #1	Si MOSFET #2	Si MOSFET #3
Number of	4	5.1	3.8	2.6
$C_{iss} \text{ (pF)}$	1920	24480	19760	13000
$C_{oss} \text{ (pF)}$	1080	1530	1330	1040
Output Charge, $Q_{oss} \text{ (nC)}$	160	370	576	421
Drive loss (W)	0.005	0.23	0.19	0.085

Table 3.4 shows the comparison of the EPC2010 to Si MOSFET with similar size (normalized to an on-resistance of 4.5 m Ω). Drive losses are calculated at a switching frequency of 50 kHz.

Even though the output capacitance of the EPC2010 is comparable to conventional Si MOSFET, the output charge is 2-4 times smaller than the Si counterparts, which indicates that the switching losses can be reduced proportionally. GaN FETs also have a very low gate drive losses due to the small input capacitance (C_{iss}) and low gate drive voltage.

Some of the design considerations in paralleling of GaN FETs are discussed below.

Parasitic inductance in the circuit has a crucial role in parallel operation; it has to be reduced in all means, even in package. GaN FETs from EPC has a LGA (Land Grid Array) package, which has an inductance of only 0.2nH [53]. A proper PCB layout is also necessary to reduce the parasitic elements of the circuit.

Individual gate drivers are recommended for each parallel FET since they eliminate the problems created by source inductance between the parallel devices in the layout, but this has some limitations. Firstly, this solution is not cost effective. Secondly, the propagation delay varies with each driver and this will make uneven turn-on and turn-off the device [51], [53]. The gate driver should be placed as close as possible to the switches to reduce the gate line inductance. It is highly recommended to add individual turn-on and turn-off gate resistors for each GaN FETs, because they help in reducing the ringing at the gate of individual FETs.

In this thesis, two different variations in layouts are considered for paralleling of four GaN FETs. As an example, the current flow in the top switch, S1.1 in a half bridge configuration when it is turned-on is shown in Fig. 3.13. This current flow is visualized in two layouts and presented in Fig. 3.15 and Fig. 3.16.

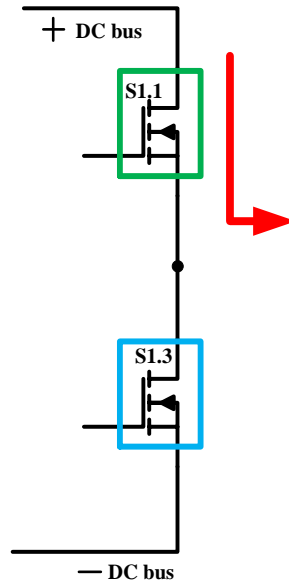


Fig. 3.13. Current flow in the top switch when the device is turned-on

(a). Layout 1. (Fig. 3.14, Fig. 3.15)

The driver is placed very close to the devices in this layout. This layout will also have low drain/source inductance since the two top and bottom layers of PCB are connected firmly using vias. The current enters or leaves the FETs through the entire width of the transformer copper foil. However, there will be a small bottle-neck created at the end at the parallel device since only half the width of copper foil is used to place the four parallel FETs.

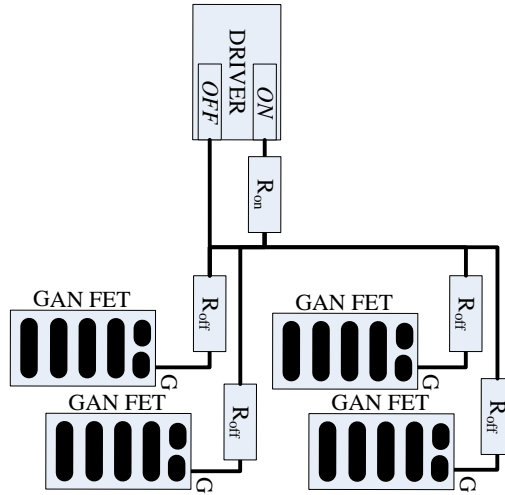


Fig. 3.14. Driver and device placement in layout 1

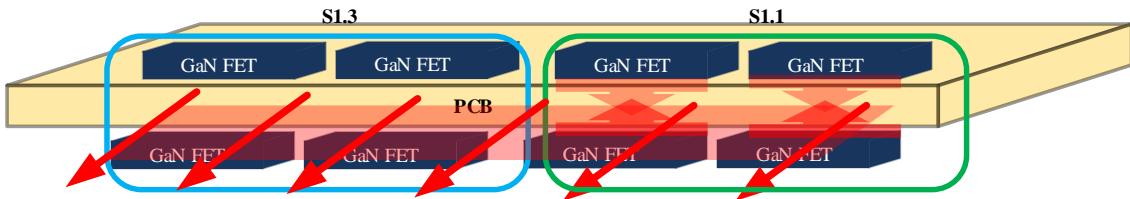


Fig. 3.15. Layout 1: two out of four parallel FETs are placed on one side of the PCB

(b). Layout 2. (Fig. 3.16, Fig. 3.17)

The distance from the drive circuit is a little longer than the layout 1. The entire width of the copper foil can be used by the current to reach the devices in parallel. This avoids any bottle-neck condition as seen in layout 1. This layout also has a comparatively higher drain/source inductance than layout 1.

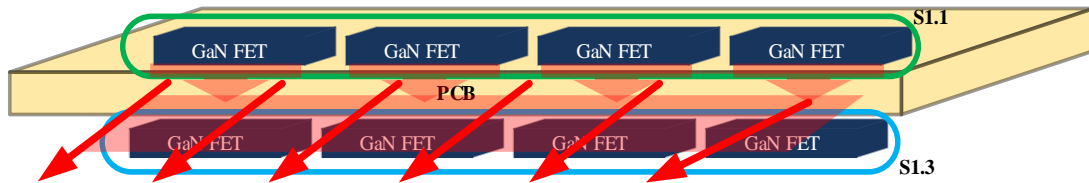


Fig. 3.16. Layout 2: four parallel FETs are placed on one side of the PCB

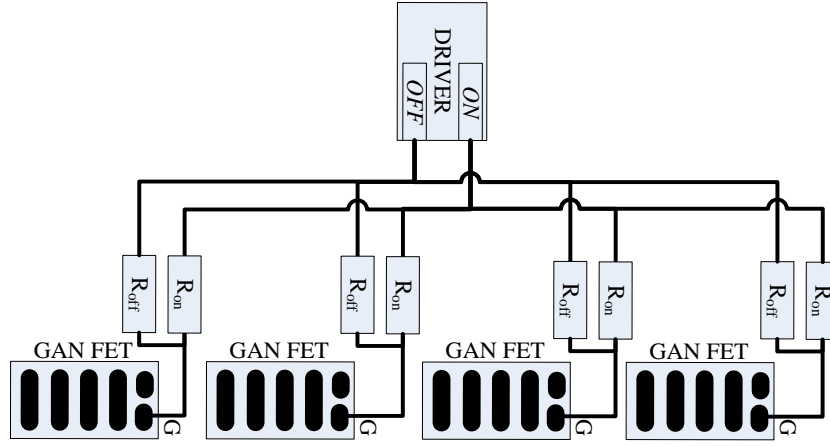


Fig. 3.17. Driver and device placement in layout 2

Since, it is extremely hard to come to a conclusion which layout is the best, two different PCBs with both the above mentioned layouts has been manufactured and tested the performance of the whole circuit. Layout 1 is used to realize converter specified in chapter 3 and Layout 2 is used in converter mentioned in chapter 4 and chapter 5.

3.3.3.3. Loss Modeling

The losses in the semiconductor device include both switching loss and conduction loss. Gate drive loss, which is directly proportional to the gate charge and the drive voltage, is also included in the switching loss. Conduction loss is dependent on the on-resistance of the switching device and the current flowing through them.

The turn-on and turn-off behavior of the MOSFET in a step down dc-dc converter is shown in Fig. 3.18.

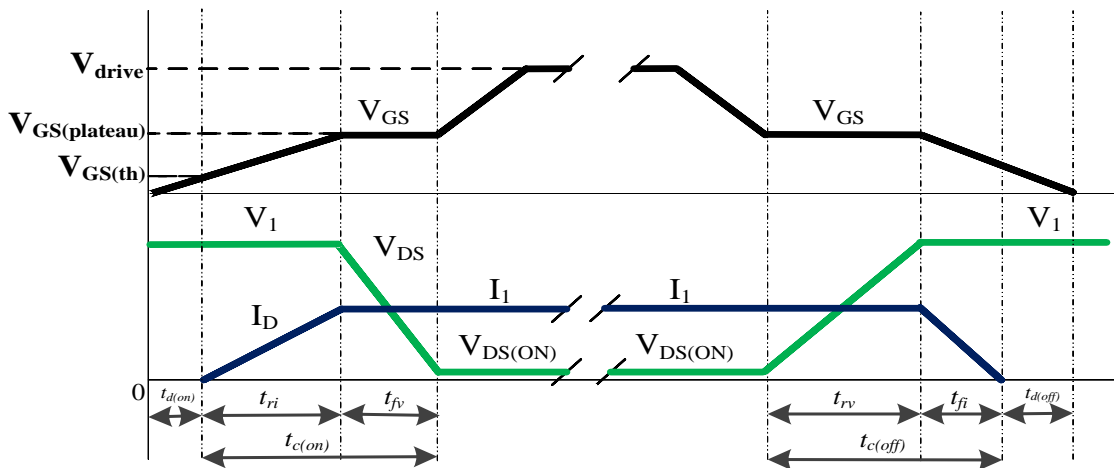


Fig. 3.18. MOSFET turn-on and turn off waveforms

During one complete switching period, the switching loss is given by,

$$P_{sw(loss)} = \frac{1}{2} V_1 I_1 [tc(on) + tc(off)] f_{sw} \quad (3.24)$$

The switching characteristics of GaN FETs along with the experimental waveforms are published as a conference paper [A3].

During each switching interval, the output capacitance of the device is charged or discharged, this energy loss constitute the major portion of switching losses in a power converter. In order to estimate the capacitive switching loss in an isolated dc-dc converter, a complete analysis is carried out and presented in Appendix [A4]. It has to be noted that at any time instant, when none of the primary switches are conducting, the output capacitance of the top primary switches is charged to $\frac{5V_{in}}{8}$ and bottom primary switches to $\frac{3V_{in}}{8}$, where $\frac{V_{in}}{8}$ is the common mode voltage across the primary switches [65]. In order to verify this voltage, the voltage across the primary top switch S1.1 and bottom switch S1.2 is measured and presented in Fig. 3.19.

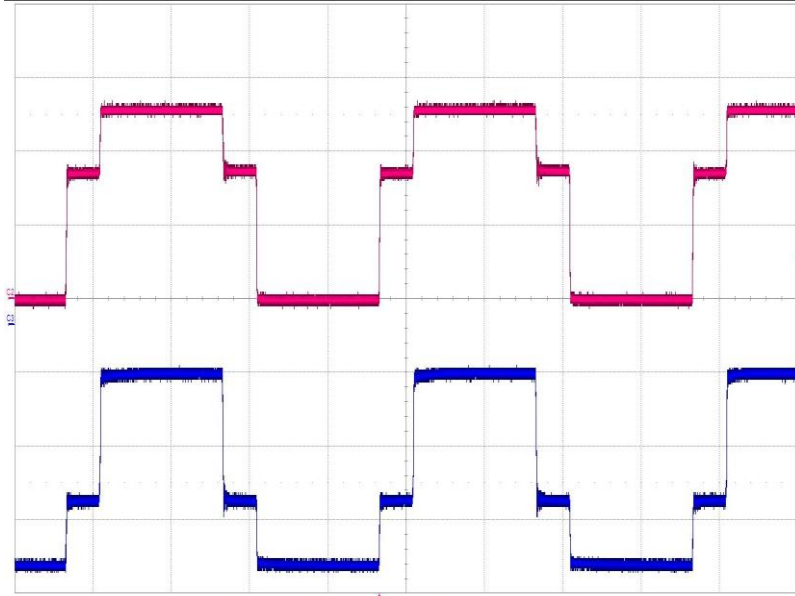


Fig. 3.19. Voltage waveform across the primary switches S1.1 and S1.2

(Red: Voltage across switch S1.1- 50V/div, Blue: Voltage across switch S1.2- 50V/div, Time: 5μS/div)

Considering the capacitive losses from all the switching devices, total capacitive switching loss for an isolated dc-dc converter can be expressed by the equation as a function of switching frequency and input voltage as [A4]

$$P_{cap(loss)} = \left\{ 2Q_{oss,p(V_{in})} - \left[\frac{5}{8} Q_{oss,p(\frac{3V_{in}}{8})} + \frac{3}{8} Q_{oss,p(\frac{5V_{in}}{8})} \right] + \frac{2}{n} Q_{oss,s(\frac{V_{in}}{n})} \right\} V_{in} f_{sw} \quad (3.25)$$

where, $Q_{oss,p(V_{in})}$ is the output charge of four parallel primary switches at V_{in} , $Q_{oss,p(\frac{5V_{in}}{8})}$ is the output charge of four parallel primary switches at $\frac{5V_{in}}{8}$, $Q_{oss,p(\frac{3V_{in}}{8})}$ is the output charge of four parallel primary switches at $\frac{3V_{in}}{8}$, $Q_{oss,s(\frac{V_{in}}{n})}$ is the output charge at $\frac{V_{in}}{n}$ of four parallel secondary switches, V_{in} is the input voltage of the converter, f_{sw} is switching frequency, and n is the transformer turns ratio.

Another major part of switching loss in a power semiconductor device is the reverse recovery losses. As far as GaN devices are concerned, the losses from reverse recovery is almost zero. This will be highly beneficial to increase the efficiency of the switching device in high current low voltage synchronous rectification applications.

The other major contribution from GaN devices is the conduction losses. In order to estimate the conduction losses RMS current through primary and secondary switches of the converter and the on-resistance of the devices are required.

The current waveforms in the primary and secondary switches are given in Fig. 3.20.

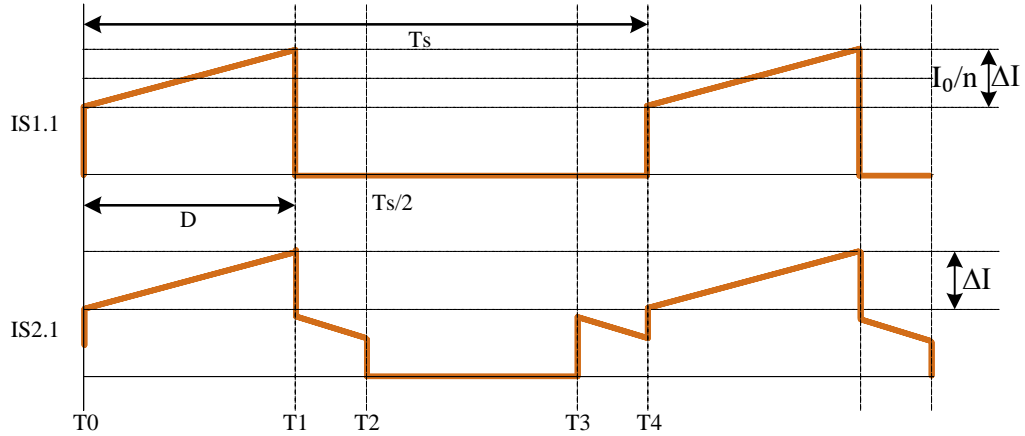


Fig. 3.20. Primary and secondary device current waveforms for an isolated dc-dc buck converter

The RMS current in the primary and secondary switches can be given by the expression (3.26) and (3.27) respectively,

$$I_{RMS,pri} = \frac{I_o}{n} \sqrt{D \left[1 + \frac{1}{12} \left(\frac{n \Delta I}{I_o} \right)^2 \right]} \quad (3.26)$$

$$I_{RMS,sec} = \frac{I_o}{2\sqrt{2}} \sqrt{\left[1 + 6D + \frac{1}{48} \left(\frac{\Delta I}{I_o} \right)^2 (1 + 30D) \right]} \quad (3.27)$$

The corresponding conduction losses in the switches are given by:

$$P_{GaN,pri} = I_{RMS,pri}^2 R_{DS(ON),pri} \quad (3.28)$$

$$P_{GaN,sec} = I_{RMS,sec}^2 R_{DS(ON),sec} \quad (3.29)$$

where, $R_{DS(ON),pri}$ and $R_{DS(ON),sec}$ are the on- resistance of primary devices and secondary devices respectively.

There is a short time interval at each switching instant when none of the secondary switches are conducting, or the ‘body diode’ of the GaN FETs is conducting. This period is called the dead-time interval. In order to have higher converter efficiency, the dead time should be minimized as much as possible. The losses during this interval can be modelled by a fixed voltage drop, V_F and a resistive element, R_D in series with V_F .

$$P_{diode} = V_F I_{D(avg)} + R_D I_{D(RMS)}^2 \quad (3.30)$$

where, $I_{D(avg)}$ and $I_{D(RMS)}$ are the average and RMS current through the ‘body diode’ of GaN FET.

The loss modelling for the switching device can be also expressed by a second order quadratic equation, as a function of output current, I_o

$$P_{GaN} = k_{GaN,o} + k_{GaN,1} I_o + k_{GaN,2} I_o^2 \quad (3.31)$$

$$k_{GaN,o} = P_{cap(loss)} + P_{drive} \quad (3.32)$$

$$k_{GaN,1} = \frac{P_{diode}}{I_o} \quad (3.33)$$

$$k_{GaN,2} = \frac{P_{GaN,pri} + P_{GaN,sec}}{I_o^2} \quad (3.34)$$

The above loss modelling of the power semiconductor device can be used to find the optimum number of devices in parallel for a given power level. In order to illustrate how the efficiency of the switching devices varies with the number of parallel devices, EPC2010 GaN FETs are considered at the primary side and EPC2001 are used at the secondary side of the converter. The capacitive losses and conduction losses are calculated for various numbers of devices in parallel and the switch efficiency curve is plotted and shown in Fig. 3.21. In case 1, 4 devices are paralleled in each switch configuration at both primary side and secondary sides of the isolation transformer. In case 2, 3 devices used in parallel at the primary side and 4 parallel devices at secondary. In case 3, 4 parallel devices at considered at the primary and 3 parallel devices at the secondary side. In case 4, 3 devices are paralleled in each switch configuration at both primary and secondary sides of the transformer. The switch efficiency curve is almost same for case 2 and case 3. In case 1 and 4, the efficiency curve is shifted with the output power level. This is obvious that for high power requirement, more devices should be used in parallel to improve the efficiency at full load but this will reduce the efficiency at light load condition.

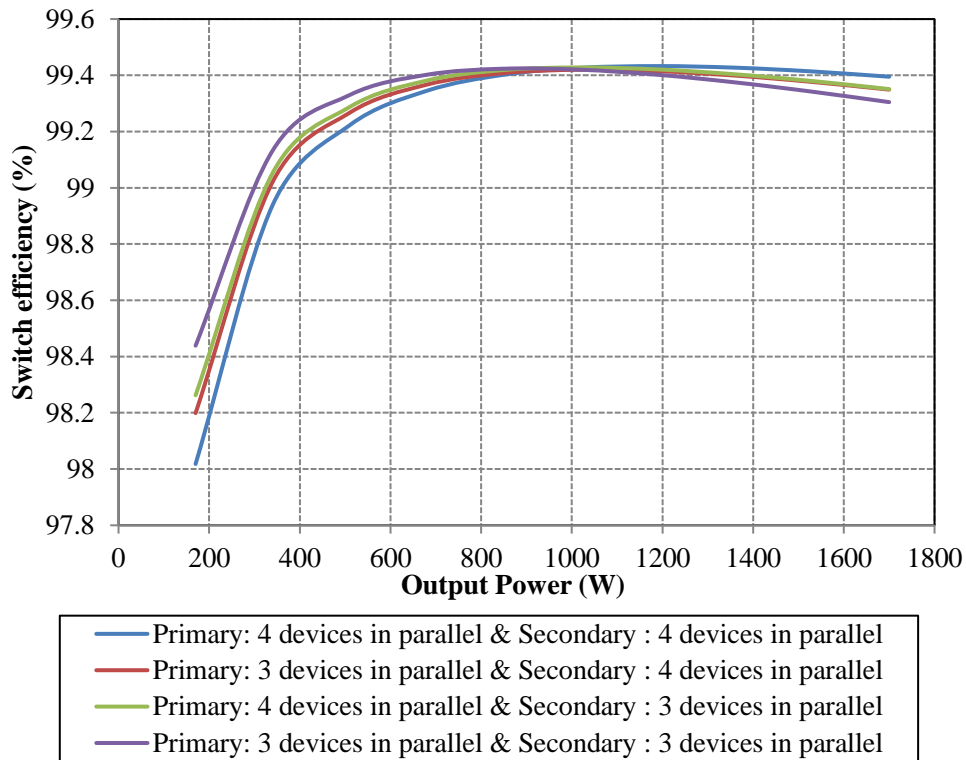


Fig. 3.21. Switch efficiency curve with various switch configurations

3.3.4. Filter Capacitor

3.3.4.1. Design Considerations

Filter capacitors are used at the input and the output sides of the converter in order to reduce the noise and the voltage ripple. The minimum value of capacitance required can be calculated

from the current through the input and output capacitors. The current waveforms for an isolated dc-dc buck converter are shown in Fig. 3.22.

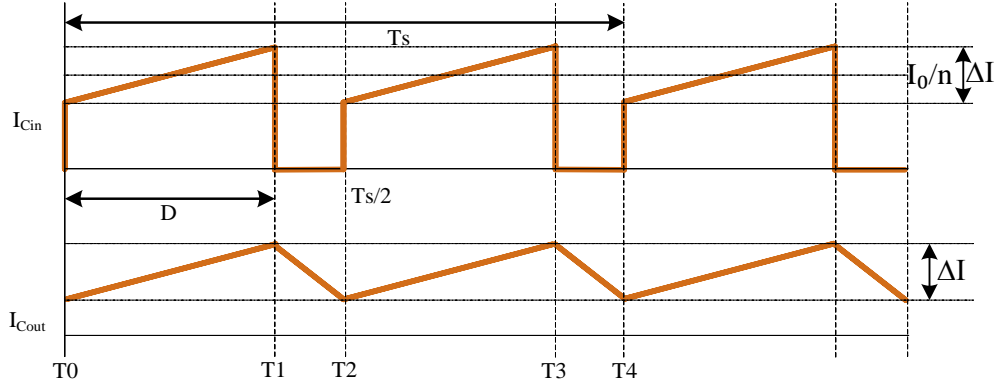


Fig. 3.22. Input and output capacitor current waveforms for an isolated dc-dc buck converter

The value of the output capacitor can be expressed by the equation

$$C_{out} \geq \frac{1}{8} \frac{\Delta I}{\Delta V_{pp}} T \quad (3.35)$$

Similarly, the input capacitance required for an isolated dc-dc converter can be written as

$$C_{in} \geq \frac{1}{n} \frac{1}{24} \frac{\Delta I}{\Delta V_{in}} (1 - D) T \quad (3.36)$$

In order to increase the power density of the converter and to reduce the dielectric losses in the filter capacitors, both input and output capacitors are realized using multilayer ceramic chip capacitors. They have a small ESR value, and thus small loss contribution. The major drawback of ceramic capacitor is the reduction of capacitance value with the dc-bias voltage. In order to reduce this effect, twice as number of capacitors required are used. This again reduces the ESR by half. This will reduce the dielectric losses associated with the filter capacitor and improve the efficiency of the converter.

3.3.4.2. Loss Calculations

The dielectric losses in the input and output capacitor can be calculated from the dissipation factor, $\tan \delta$ of the filter capacitors used. The losses in the input and output capacitors can be given by the equation,

$$P_{Cin} = \frac{I_{RMS,Cin}^2 \cdot \tan \delta_{Cin}}{4 \pi f C_{in}} \quad (3.37)$$

$$P_{Cout} = \frac{I_{RMS,Cout}^2 \cdot \tan \delta_{Cout}}{4 \pi f C_{out}} \quad (3.38)$$

where, $I_{RMS,Cin}$ and $I_{RMS,Cout}$, are the RMS current through the input and output filter capacitors, $\tan \delta_{Cin}$ and $\tan \delta_{Cout}$ are the respective dissipation factors and C_{in} and C_{out} are the respective capacitance values.

3.4. Loss Modeling for a 1.7 kW GaN Converter

The specification for an isolated dc-dc GaN converter with an output power of 1.7 kW is presented in Table 3.5.

Table 3.5: Converter specification for 1.7 kW output power

Output Power	P_o	1.7 kW
Input Voltage	V_{in}	130 V
Output Voltage	V_o	50 V
Switching Frequency	f_{sw}	50 kHz
Transformer Turns Ratio	$n:1$	2:1

Considering all the losses together from section 3.3, the power loss equation for the proposed 1.7 kW isolated dc-dc buck converter can be written as a function of output current, I_o .

$$P_{tot} = 6.81 + 0.0098 I_o + 0.0117 I_o^2 \quad (3.39)$$

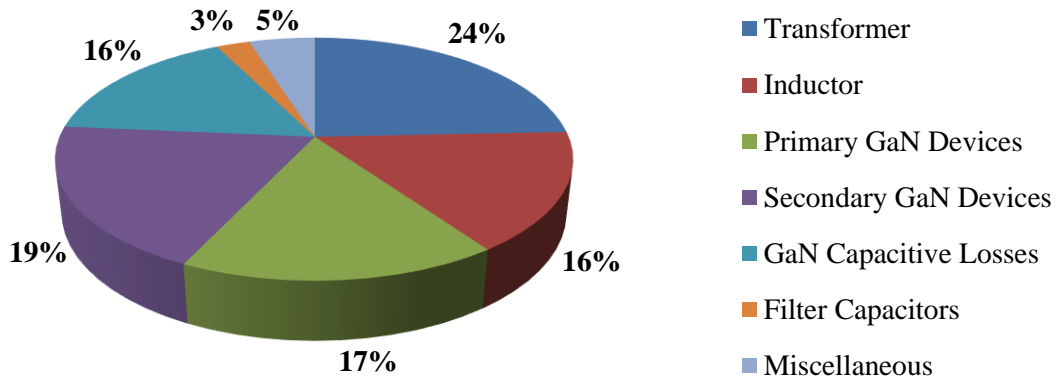


Fig. 3.23. Loss breakdown for an isolated buck converter at 1.7 kW output power

The losses in the individual power components at 1.7 kW output power are calculated and the loss distribution of the converter is plotted in Fig. 3.23. The losses in the PCB traces are not considered in the power loss calculations.

3.5. Efficiency Measurement

Before discussing the experimental results, how precisely the efficiency can be measured in a dc-dc converter is explained in this section. As converter efficiency increases, for e.g. above 95%, it is necessary to validate and accurately measure the efficiency of the converter precisely. The most popular methods used for efficiency measurement are calorimetric measurement method and voltage-current measurement method. Calorimetric method is well suited for converters with an output power of several kW's. However, it requires the proper design and calibration of the calorimetric chamber and it is not cost effective method.

On the other hand, voltage-current measurement method is a cost effective and can be used to measure the efficiency precisely, if the measurement setups are calibrated properly. In order to measure the voltage accurately, high precision digital multi-meters are used. Keysight 34410A digital multi-meters is a good choice since it has an accuracy of $\pm 0.0026\%$, considering voltage and temperature range.

However, the current measurements become more critical and challenging. High precision current sense resistors with a temperature stability of less than 1 ppm/K are used for current measurement. Shielded cables and common mode filters are used to avoid any noise injection in the measurement.

The efficiency measurement setup is shown in Fig. 3.24.

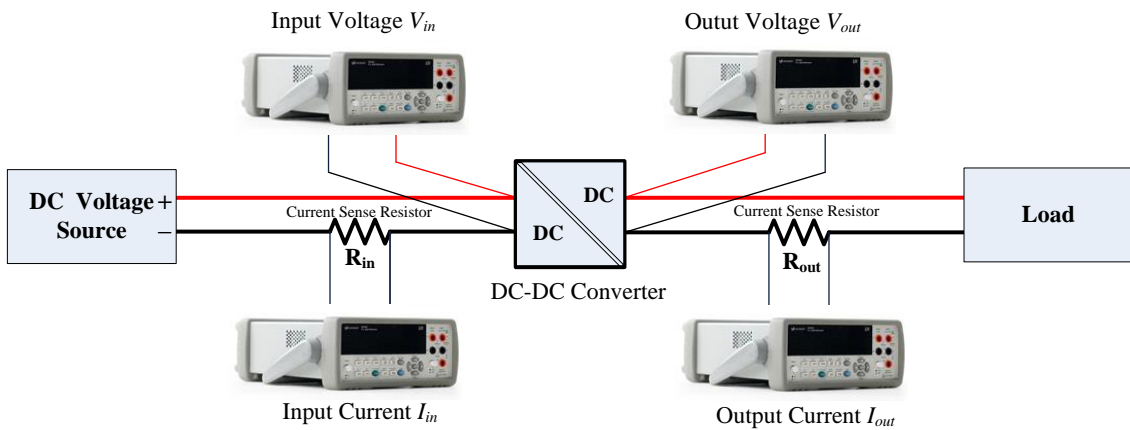


Fig. 3.24. Efficiency measurement setup for dc-dc converters

Proper calibration of the instruments and the placement of measurement points are very important to measure the efficiency precisely. Since, efficiency, η is the product of voltage and current ratio (3.40)

$$\eta = \frac{V_o}{V_{in}} \frac{I_o}{I_{in}} \quad (3.40)$$

The ratio of the deviation in the sense resistors can be measured or validated by passing the same current through them by placing them at the input or output side of the converter. This helps in calibrating the meters and measuring the values precisely. The precision of this measurement method is better than $\pm 0.1\%$ [64].

3.6. Experimental Results

The hardware prototype of the 1.7 kW isolated dc-dc buck converter is shown in Fig. 3.25. The placement of the parallel GaN FETs as layout 1 (Fig. 3.15) is shown in Fig. 3.26.

The converter is tested with an input voltage of 130V and the output is connected with an electronic load. The efficiency of the converter is measured with the same procedure as explained in section 3.5.

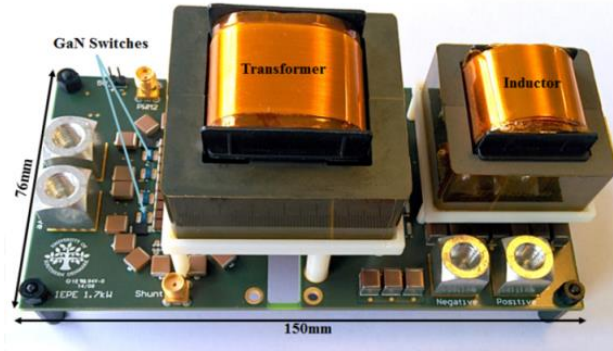


Fig. 3.25. Hardware prototype of a 1.7 kW isolated dc-dc GaN converter

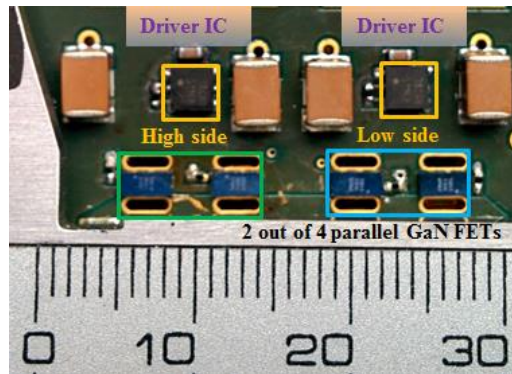


Fig. 3.26. Placement of parallel GaN FETs for the proposed 1.7 kW GaN converter

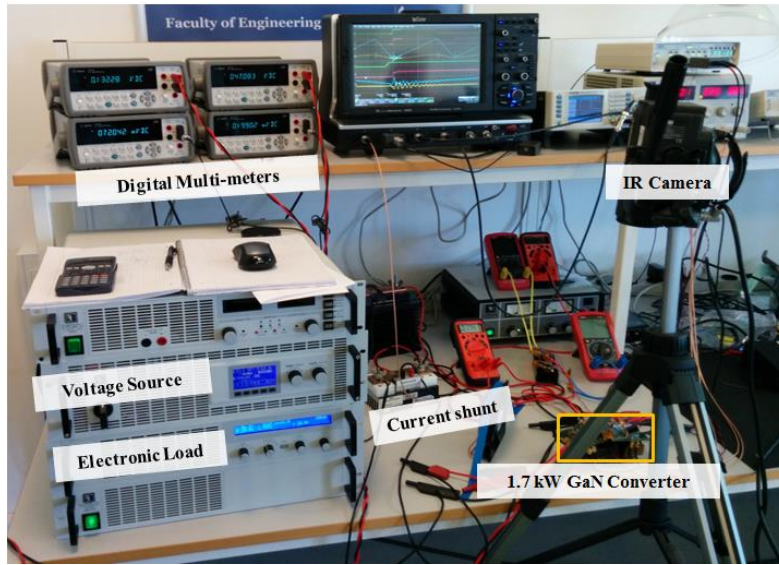


Fig. 3.27. Experimental test setup for the GaN converter

The test bench for the efficiency measurement for the converter is shown in Fig. 3.27. Measured waveforms of the GaN converter are shown in Fig. 3.28. Measured waveforms look very clean with only small ringing and limited spikes.

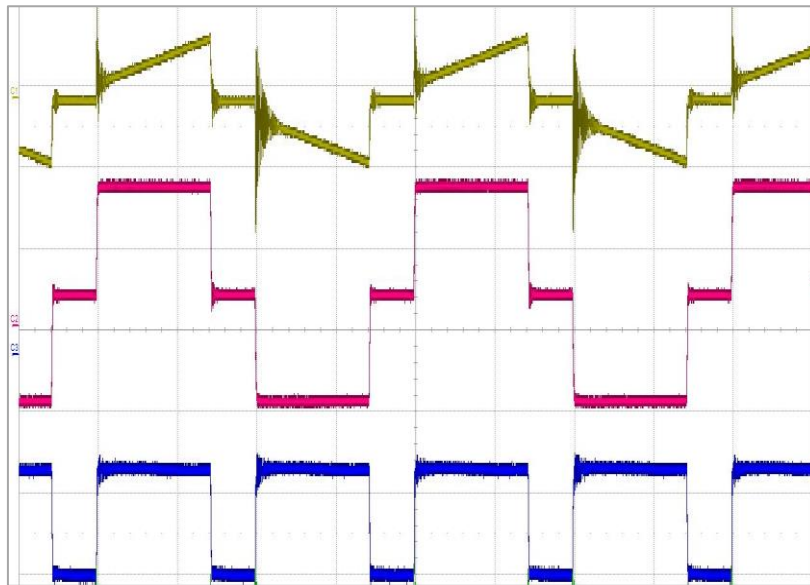


Fig. 3.28. Measured waveforms of the GaN converter

(Yellow: Transformer primary current 20A/div, Red: Transformer primary voltage 100V/div, Blue: Rectifier voltage 50V/div, Time scale: 5 μ S/div)

The current measurements in GaN FETs are extremely difficult due to their small size and the absence of any leads for the connection to the PCB. In order to avoid introducing any parasitic impedance in the circuit, an infrared camera is used to monitor the temperature of the GaN FETs. These temperature measurements will give an indication of sharing of current in the

paralleled GaN FETs. IR image of the converter using a FLIR AGEMA 570 IR camera at 1 kW output power is shown in Fig. 3.29.

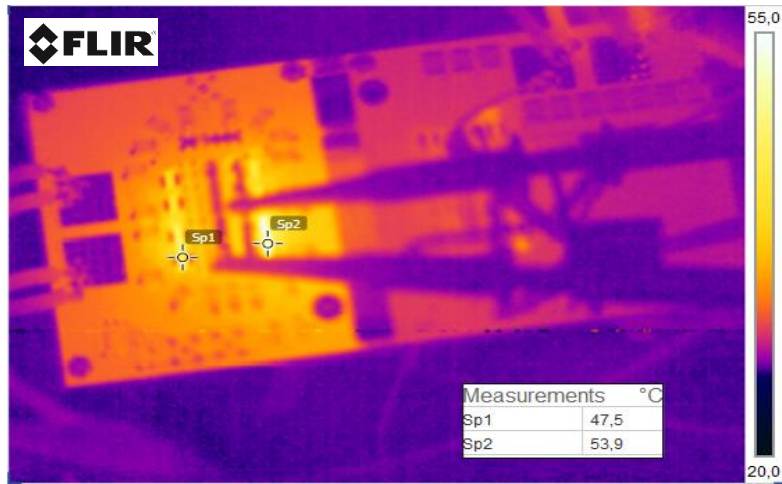


Fig. 3.29. IR image of the converter at 1 kW output power

The efficiency of the converter is measured up to 1.7 kW output power and shown in Fig. 3.30. The gate drive loss of the converter is less than 150mW. The maximum measured efficiency of the converter is 98.5% at approximately 1 kW output power. Since the maximum efficiency of the converter occurs at 1 kW, the ‘comparative’ power rating of the converter can be referred as 2 kW. The converter has an efficiency of 98.3% at an output power of 1.7 kW.

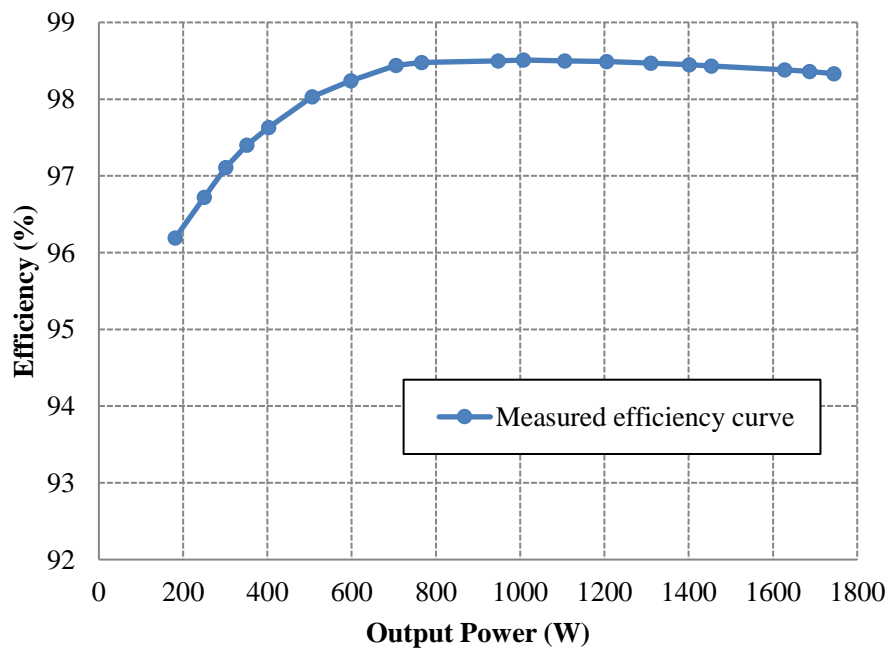


Fig. 3.30. Measured efficiency curve of the 1.7 kW isolated dc-dc GaN converter

3.7. Conclusion

This chapter has focused on the loss modelling of an isolated dc-dc GaN converter. In order to improve the efficiency of the converter, the efficiency of the individual power components has to be increased. Various approaches for the improvement of efficiency in magnetics are also discussed in this chapter.

- In transformer, extensive interleaving of primary and secondary winding results in very low ac-resistance. Interleaving of the windings and low number of turns will reduce the transformer leakage inductance and hence reduces the stored leakage energy.
- Two winding inductor design will significantly reduce the ac-winding losses in high current high power inductors.

Due to the superior material properties of GaN devices compared to Si MOSFET, they can be used in power converters to make them more efficient and compact. The conduction losses from the power semiconductor devices can be reduced by paralleling the devices. The chapter has also discussed on various considerations in paralleling of GaN FETs for an isolated dc-dc converter. Even though the gate drive losses are almost negligible for GaN FETs, the capacitive switching loss will increase with the paralleling of devices. Therefore, an optimum number of the parallel devices has to be selected in order to have a trade-off between the conduction losses and the switching losses.

Proper layout is another vital requirement to achieve high efficiency. Parasitic impedance has to be reduced as much as possible. Even though this will make the measurement of current in the circuit much difficult, an IR camera can be used to sense the temperature of the devices, thereby estimating the current sharing.

Further, this chapter has demonstrated the hardware prototype of a 1.7 kW GaN converter. The converter is tested with an input voltage of 130V and the measured efficiency curve of the converter is presented in this chapter. The maximum measured conversion efficiency of the converter is 98.5% at 1kW of output power.

4. Phase Shifted Isolated DC-DC Converter

From the loss modelling of the converter in the previous chapter, around 16% of total power losses are from the device output capacitance. The objective of this chapter is to realize a zero voltage switching isolated dc-dc converter to regain the capacitive switching loss. Many of the converters in literature cannot obtain ZVS at light load condition. This is mainly due to the reason that traditional ZVS isolated converters rely on the energy stored in transformer leakage inductance or an inductor in series with the transformer to provide ZVS for the primary switches [66], [67].

The method explained in this chapter uses magnetizing current to achieve ZVS of the primary switches. This helps in achieving ZVS even at light load condition. The same magnetics for isolated dc-dc stepdown converter as explained in chapter 3 are used to realize the phase-shifted isolated dc-dc converter. The analyses of the converter along with the experimental results are presented in this chapter.

A conference paper has also been published based on this topic [A2].

4.1. Operation of a Phase Shifted Isolated DC-DC Converter

The circuit diagram for an isolated phase shifted dc-dc converter is shown in Fig. 4.1. Fig. 4.2 shows the timing diagram along with the operational waveforms of the converter. In Fig. 4.2, V_{Tl} is the transformer primary voltage, T_s is the switching period, ΔI is the inductor ripple current, I_{Lm} is the transformer magnetizing current, I_{Ll} is the inductor current and V_{Ll} is the inductor voltage.

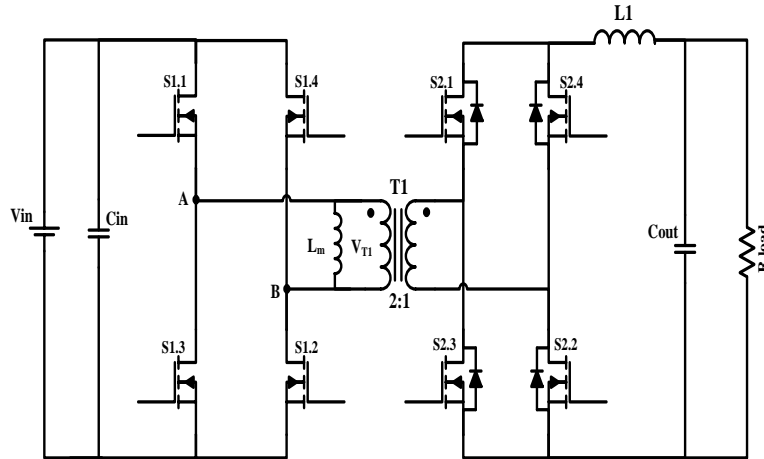


Fig. 4.1. Schematic diagram of a phase shifted full bridge isolated dc-dc converter

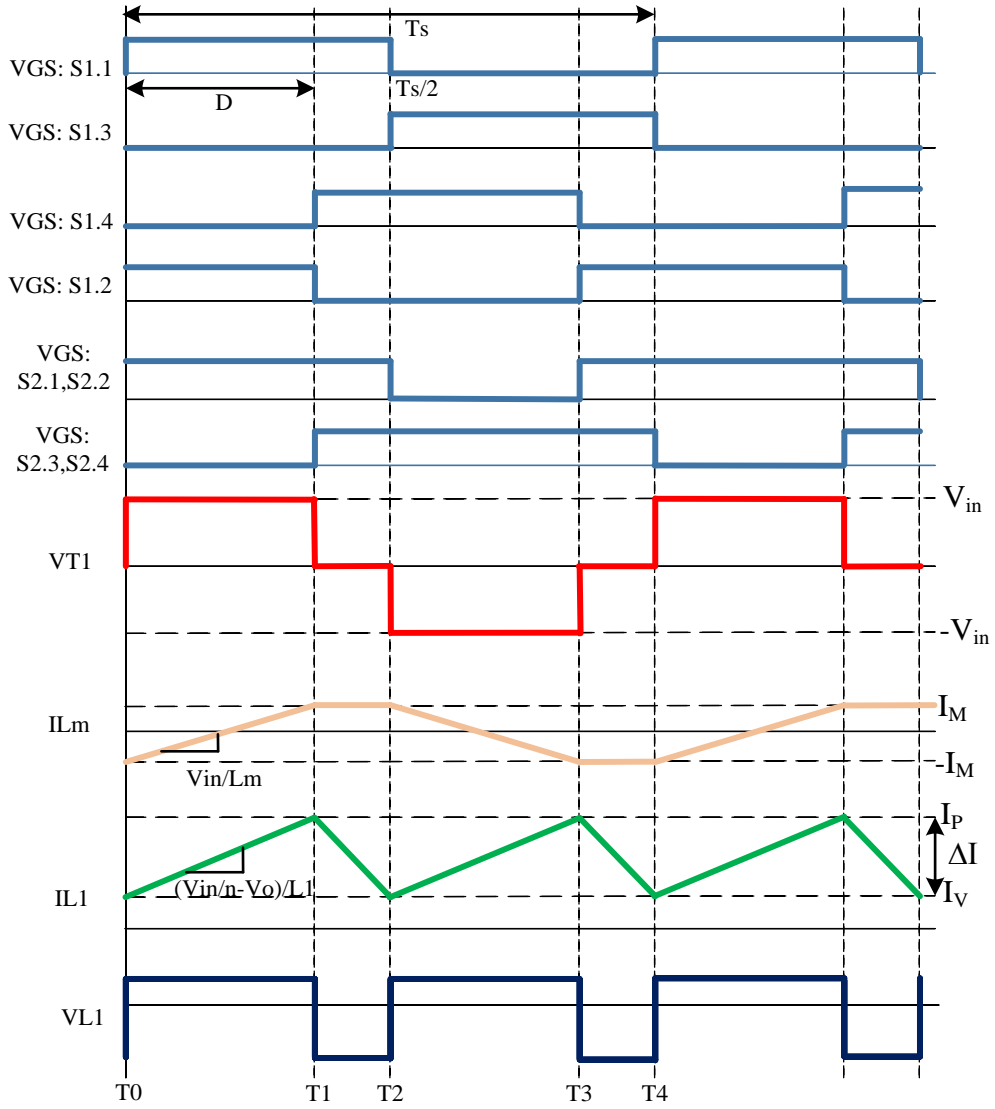


Fig. 4.2. Operational waveforms of a phase shifted isolated dc-dc converter

The operation of the phase shifted isolated dc-dc converter can be divided into four intervals- two power transfer intervals and two freewheeling intervals.

A. Time interval between T_0 - T_1

During this interval of time, diagonal switches $S_{1.1}$ and $S_{1.2}$ are turned on. On the secondary side of the converter, switches $S_{2.1}$ and $S_{2.2}$ will conduct and the inductor L_1 is charging with a slope $\frac{(V_{in}/n - V_o)}{L_1}$, where V_{in} is the input voltage and V_o is the output voltage. This stage is called the power transfer stage, since the power will be transferred from input to output during this interval.

B. Time interval between T1-T2

Switch S1.2 is turned off and output capacitor of the device is charged commutating the voltage at A. The magnetizing current forward biases the diode across S1.4, clamping the voltage to conduct before the switch is turned on. Thereby the switch S1.4 is turned on at zero voltage. This interval of time is called the freewheeling stage. There is no power transfer during this interval. The secondary side of the transformer is shorted and the inductor current freewheels in the secondary switches.

C. Time interval between T2-T3

This interval is also a power transfer stage, during which the diagonal switches S1.4 and S1.3 conducts on the primary side and S2.4 and S2.3 conducts on the secondary side of the converter. The switches on the primary side are turned-on for a period of DT_s . Reflected inductor current flows from the input capacitor, C_{in} through switch S1.4, transformer T1, switch S2.4, inductor, L1 to the output and the current returns through the switches S2.3 and S1.3 to the input.

D. Time interval between T3-T4

This interval is similar to time interval between T1-T2. Zero voltage switching occurs for switch S1.2. During this period, magnetizing current circulates through S1.3 and S1.2. Secondary side of the transformer is shorted and the inductor current freewheels in the secondary switches of the converter. This interval is also called the freewheeling stage.

The output voltage of the isolated phase shifted dc-dc converter is given by

$$V_o = \frac{2}{n} D V_{in} \quad (4.1)$$

4.2. Analysis of a Phase Shifted Isolated DC-DC Converter

As explained in loss modelling, in any power converters, idle losses dominate the power losses at light load condition i.e. the percentage of switching losses among the total losses in the converter is bigger. Therefore, it is desirable to achieve zero voltage switching at light load conditions. The magnetizing current in the transformer can be used to achieve ZVS of the primary switches at no load and light conditions.

The input voltage V_{in} , will be available across the transformer primary winding when the diagonal switches at the primary side are turned-on (neglecting the voltage drop across the switches).

The primary winding voltage, $V_{Tl}(t)$, across the magnetizing inductance of the transformer L_m can be given by

$$V_{T1}(t) = L_m \frac{di_{Lm}(t)}{dt} \quad (4.2)$$

Integrating the above equation,

$$i_{Lm}(t) - i_{Lm}(0) = \frac{1}{L_m} \int_0^t V_{T1}(t) dt \quad (4.3)$$

So, the magnetizing current can be determined by integrating the applied primary winding voltage. During steady state operation, the voltage applied across the magnetizing inductance must be zero.

$$\frac{1}{T_s} \int_0^{T_s} V_{T1}(t) dt = 0 \quad (4.4)$$

The magnetizing current is proportional to the integral of voltage applied across the winding, so it is important that the voltage across the inductance over a complete switching period should be zero. Otherwise, the net increase in magnetizing current at each interval will eventually lead to excessive large current and saturate the transformer.

Practical transformers will have leakage inductance. The amount of leakage inductance in the transformer can be controlled by varying the coupling of primary and secondary windings. Under heavy load conditions, leakage inductance can provide the energy required for zero voltage switching. The main drawback of using magnetizing current without having much leakage inductance in the transformer is that, ZVS condition ceases when the magnetizing current is smaller than the reflected load current.

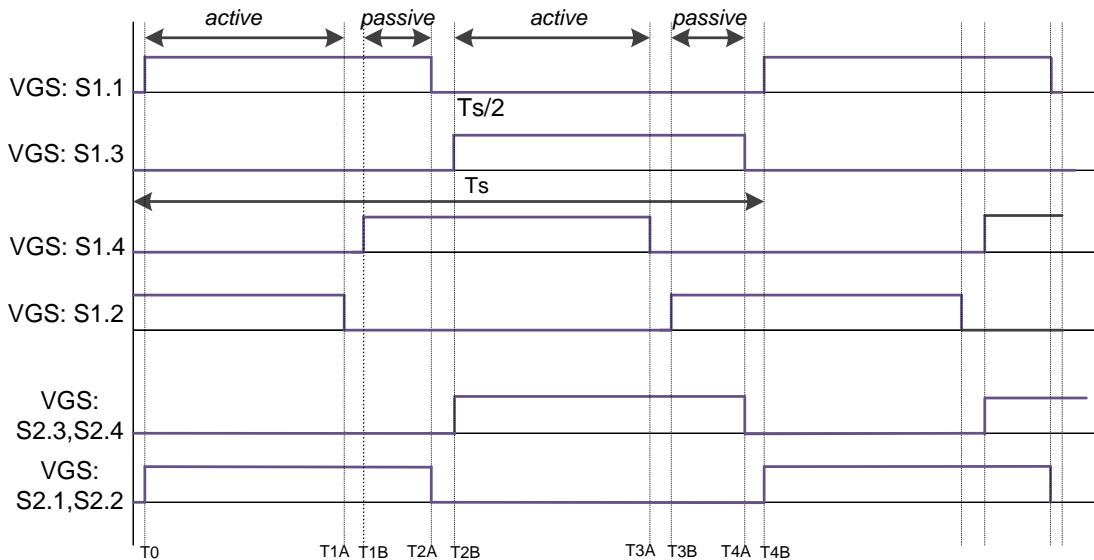


Fig. 4.3. Switching pattern for a phase shifted isolated dc-dc converter

In order to explain the reason for why ZVS condition ceases, a complete illustration of how ZVS occurs at the primary switches is required. In a phase shifted isolated dc-dc converter, enough dead time has to be provided between the switching of same leg switches to avoid cross conduction as well as to provide enough time to charge or discharge the output capacitance of the switches, before it is turned on. The exact timing diagram for the switches is shown in Fig. 4.3.

As explained in the working principle of the phase shifted isolated dc-dc converter (section 4.1), there will be four intervals during each switching period - two power transfer interval and two freewheeling interval. The power transfer interval is referred as the active stage and the freewheeling period as the passive stage. During active to passive state change, i.e. the time interval between $T1A-T1B$, the capacitance of half-bridge leg consisting of switches S1.2 and S1.4 has to be charged and discharged, respectively. The circuit operation is given in Fig. 4.4.

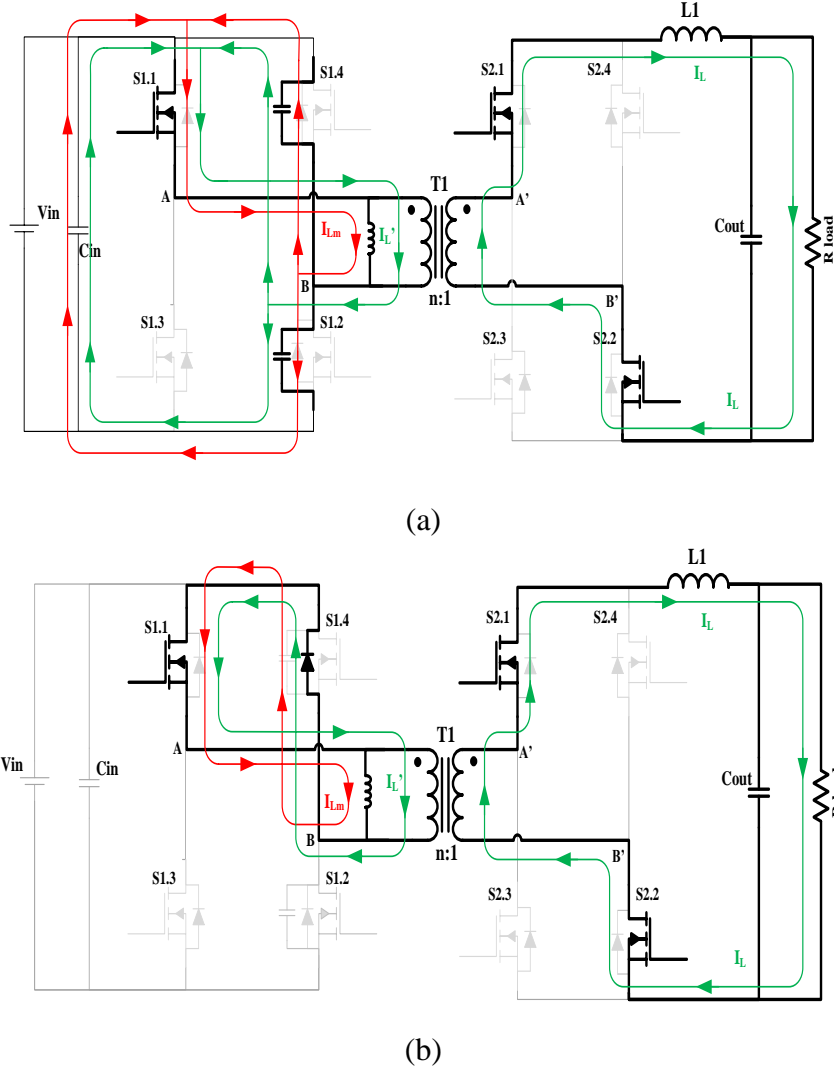


Fig. 4.4. Operation of the converter during active to passive transition

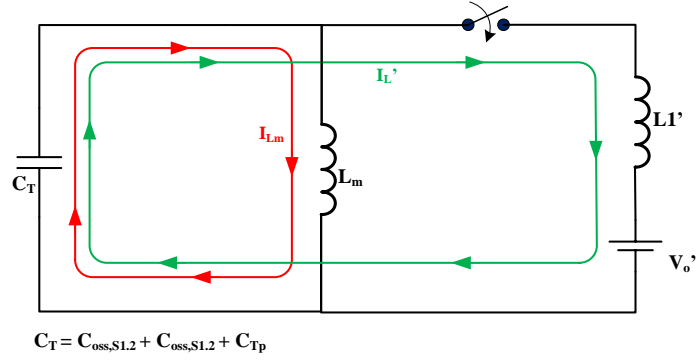


Fig. 4.5. Equivalent circuit during active to passive transition

The equivalent circuit during the transition from active to passive stage is shown in Fig. 4.5. In the circuit, I_L' is the primary reflected inductor current, C_T is the sum of output capacitance of two switches and the transformer winding capacitance. From the equivalent circuit, it is seen that the output capacitance of the switches will be charged and discharged by the magnetizing current as well as the reflected inductor current.

During the freewheeling or the passive stage, all the switches in the secondary side are conducting. The magnetizing current can flow through primary winding or secondary winding or divide between primary and secondary windings. The division of magnetizing current depends on the conducting transistor characteristics and the leakage inductance in the circuit. The circuit operation of the converter during passive stage is shown in Fig. 4.6.

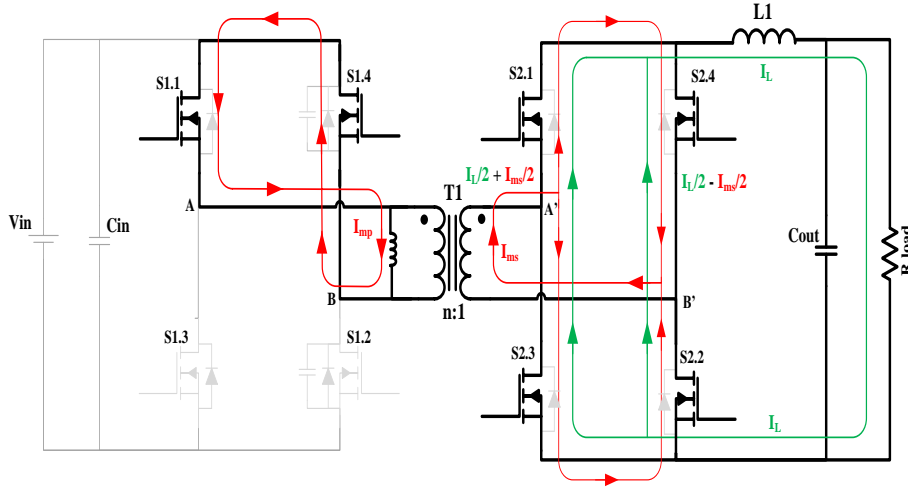


Fig. 4.6. Operation of the converter during passive stage

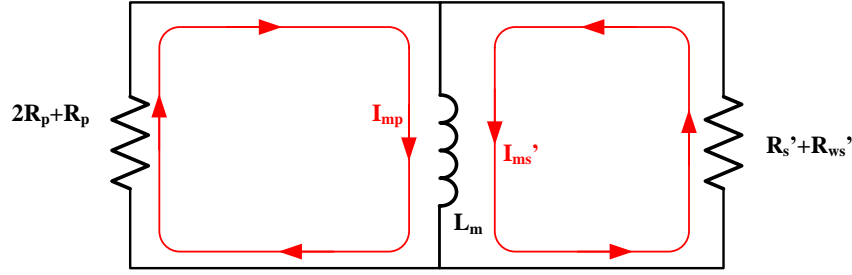


Fig. 4.7. Equivalent circuit showing division of magnetizing current during passive stage

The division of magnetizing current in the primary and secondary sides of the converter depends on the impedance of the respective circuit. The equivalent circuit is shown in Fig. 4.7. The leakage inductance of the transformer can be neglected for the designed transformer, as it is extremely small. The sharing of magnetizing current can be defined as

$$I_{mp} = \frac{R_s' + R_{ws}'}{2R_p + R_s' + R_{ws}'} I_M \quad (4.5)$$

$$I_{ms}' = \frac{2R_p + R_p}{2R_p + R_{wp} + R_s' + R_{ws}'} I_M \quad (4.6)$$

$$I_{ms} = n I_{ms}' \quad (4.7)$$

where, I_M is the peak value of magnetizing current, n is transformer turns ratio, R_p and R_{wp} are the on-resistance of the primary MOSFET and transformer primary winding resistance respectively. R_s' and R_{ws}' are the secondary MOSFET on-resistance and transformer secondary winding resistance referred to primary side of the transformer.

The current through the secondary side transistors are functions of both magnetizing current and load current. The current through the switches S2.1 and S2.2 can be written as

$$i_{S2.1}(t) = i_{S2.2}(t) = \frac{I_L(t)}{2} \pm \frac{I_{ms}}{2} \quad (4.8)$$

Then the current through switches S2.3 and S2.4 can be

$$i_{S2.3}(t) = i_{S2.4}(t) = \frac{I_L(t)}{2} \mp \frac{I_{ms}}{2} \quad (4.9)$$

The converter operation during the passive to active stage is shown in Fig. 4.8. During this instant, the magnetizing current will be opposed by the reflected load current and the net current will be only available to discharge the output capacitance of switch S1.3. The equivalent circuit of the converter during this instant of time is shown in Fig. 4.9.

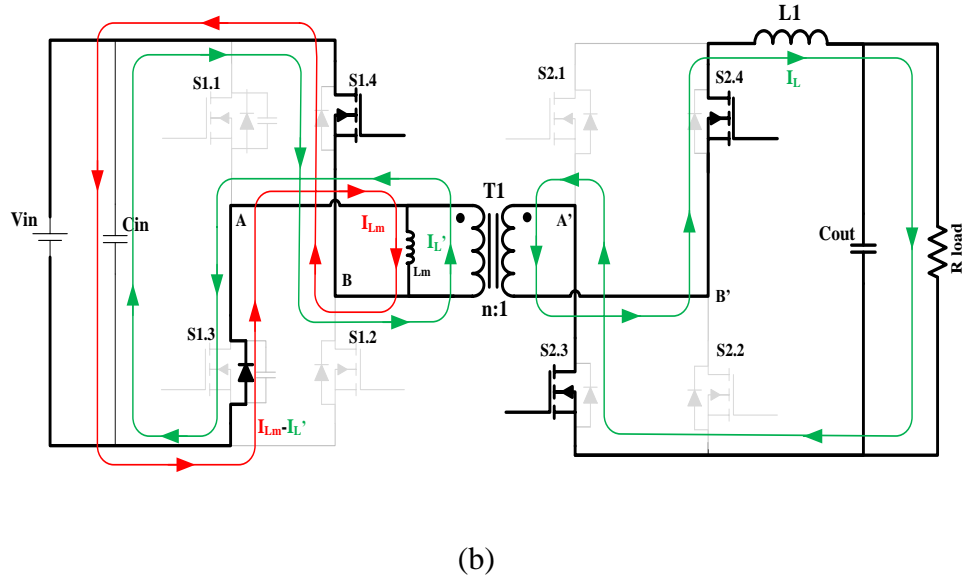
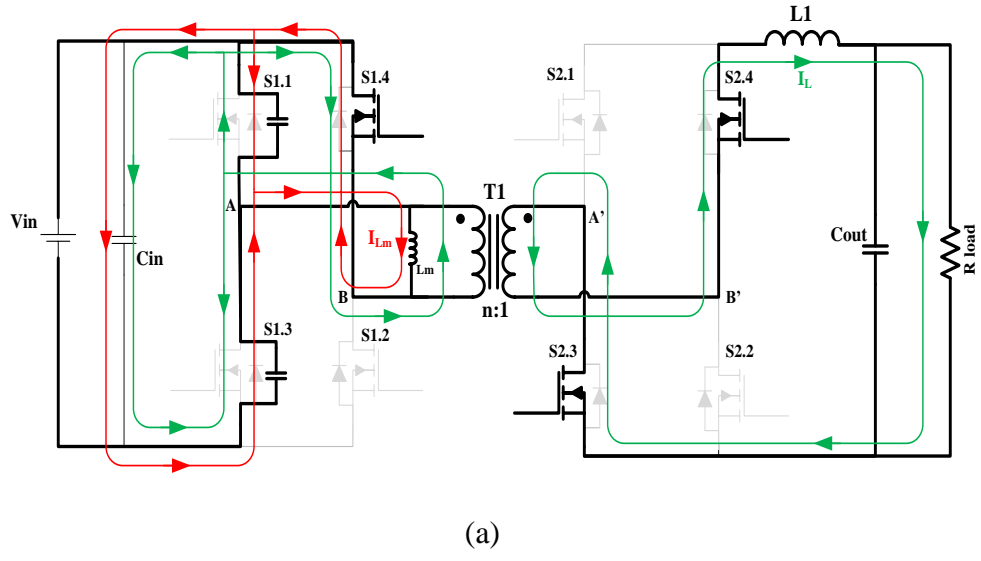


Fig. 4.8. Operation of the converter during passive to active transition

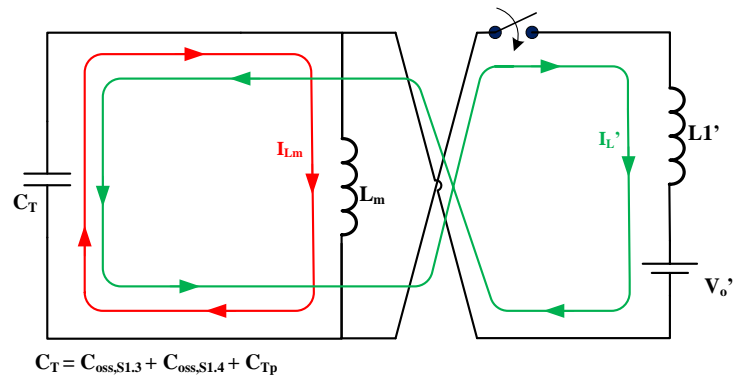


Fig. 4.9. Equivalent circuit during passive to active transition

The same sequence of circuit operation will repeat once again before the next switching period starts. Therefore, the output capacitance of switches S1.2 and S1.4 can be easily charged and discharged at all load conditions, since both the magnetizing current and reflected current aids this process. However, during the charging and discharging of output capacitance of switches S1.1 and S1.3, reflected load current opposes the magnetizing current and only the net current will be available. Hence, when the reflected load current is larger than the magnetizing current, ZVS of switches S1.1 and S1.3 ceases and switches will be hard-switched thereafter.

4.3. Design Considerations

The design considerations for the phase shifted dc-dc converter remains the same as chapter 3, except that an airgap is introduced in the transformer core. An airgap in the core reduces the magnetizing inductance of the transformer. This will increase the magnetizing current, which is used to achieve zero voltage switching at the primary switches. Losses from the magnetizing current are inevitable but this will help in providing ZVS switching even at no load.

An optimum value of magnetizing inductance has to be selected to have a tradeoff between conduction losses from the magnetizing current and the ‘comparative’ power rating of the converter.

4.4. Experimental Results

The hardware prototype of a full bridge isolated phase shifted dc-dc converter is shown in Fig. 4.10.

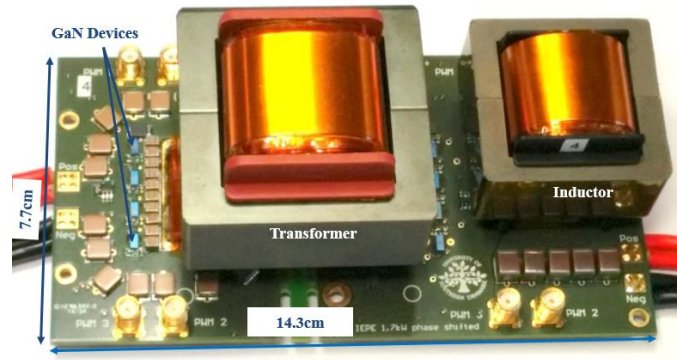


Fig. 4.10. Hardware prototype of a phase shifted isolated dc-dc converter

The measured waveforms of the converter are shown in Fig. 4.11. As mention in the earlier chapter, the current measurement is almost impossible without being adding any parasitic in the circuit. An infrared camera from Avio with a resolution of 320 x 240 pixels is used to monitor the GaN FETs. The image from the IR camera at 800W is shown in Fig. 4.12.

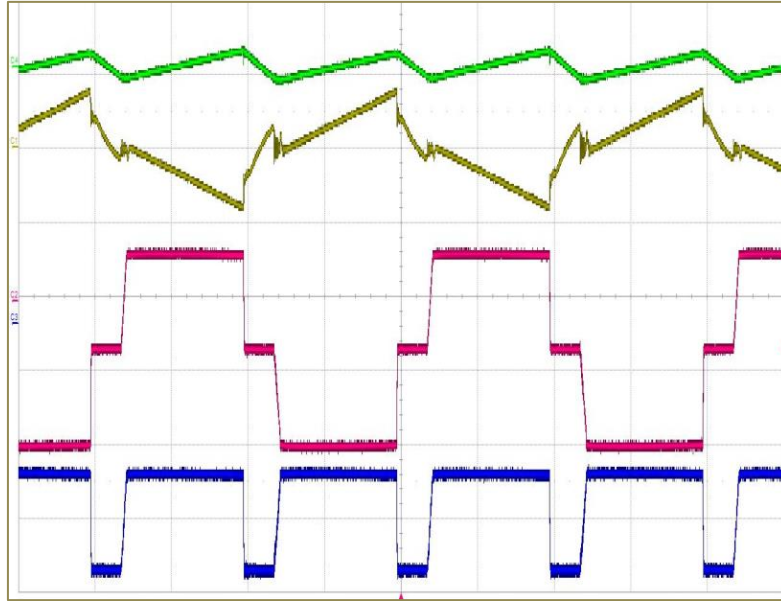


Fig. 4.11. Various measured waveforms of the phase shifted dc-dc converter (Green: Inductor current 20A/div, Yellow: Transformer primary current 20A/div, Red : Transformer primary voltage 100V/div, Blue : Rectifier voltage 50V/div, Time : 5 μ S/div)

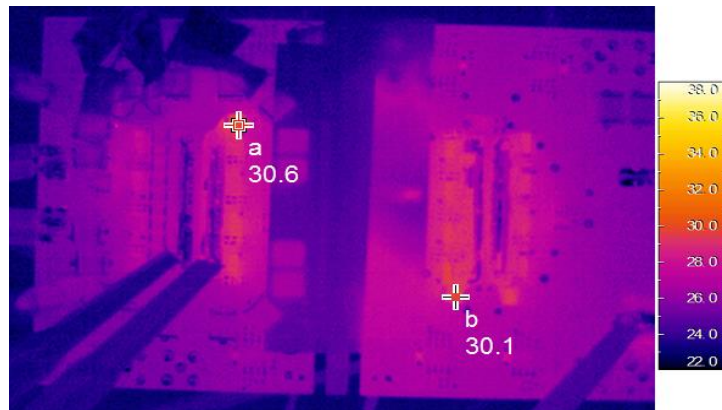


Fig. 4.12. IR image of the phase shifted dc-dc converter at 800W

The efficiency of the converter is measured precisely with a measurement tolerance of less than $\pm 0.1\%$. The efficiency of the phase-shifted converter is measured for various values of magnetizing inductance and shown in Fig. 4.13. As the magnetizing current is increased, the ‘comparative’ power rating of the converter can be increased, but the efficiency of the converter reduces. From the figure, it is clear that with the increase of magnetizing current, power density of the converter can be increased, but the conduction loss from the circulating magnetizing current at the primary switches also increases and severely reduces the light load efficiency, even though it removes the switching losses.

Fig. 4.13 shows the transition of soft switching to hard switching of the primary switches as the load current is increased and becomes greater than the value of secondary reflected magnetizing current.

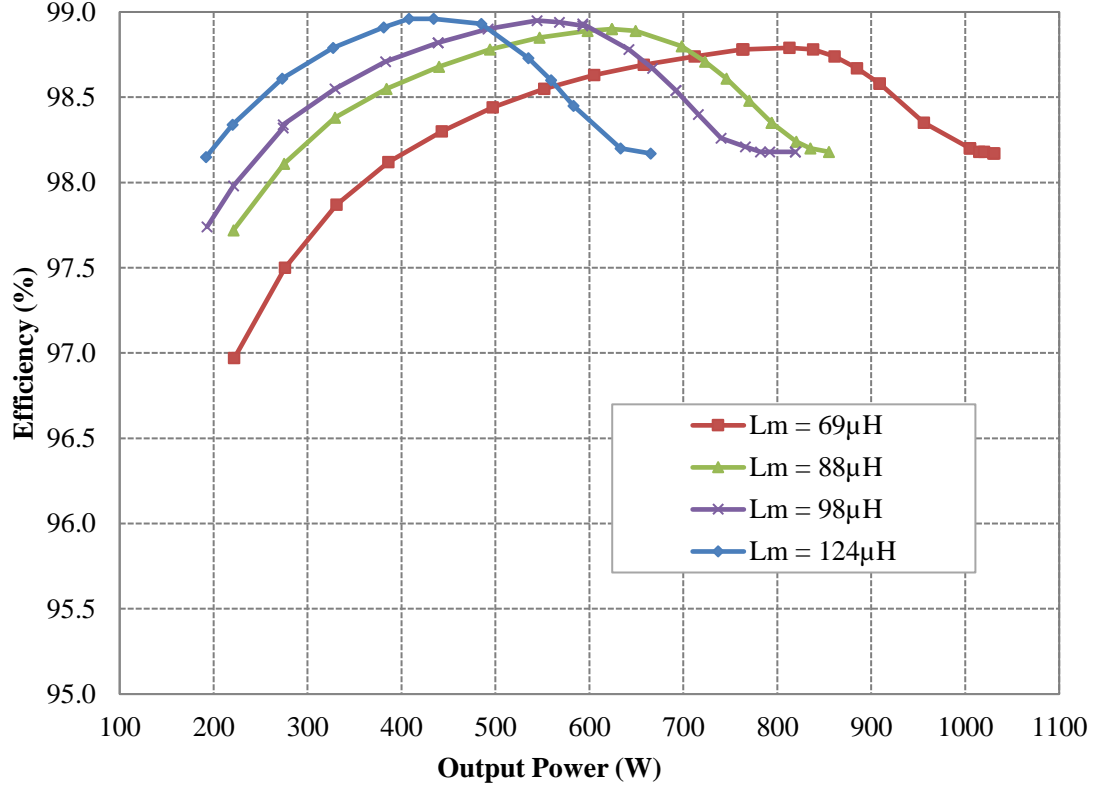


Fig. 4.13. Measured efficiency curve of the GaN converter with various magnetizing inductance

From the efficiency curve, the maximum efficiency point shifts with the variation in magnetizing inductance. Magnetizing current can be increased to improve the ‘comparative’ power rating of the converter, but this penalizes mainly the light load efficiency due to the losses from the magnetizing current, even though it eliminates the switching loss at this load condition. The peak efficiency of the phase-shifted converter is measured as 98.8% when the converter is operated to an output power of 1 kW.

4.5. Conclusion

The following conclusions can be drawn from this chapter.

- The percentage of power loss from capacitive switching loss is higher at low load conditions, so zero voltage switching using magnetizing inductance is highly

advantages. Even though this will increase the conduction losses in the device due to the magnetizing current, it ensures ZVS even at light load condition.

- The implementation of a phase shifted isolated dc-dc converter using a very low leakage transformer is presented in this chapter.
- The chapter also highlights that the switching losses in the converter can be reduced, and can be able to achieve high efficiency. However, the ‘comparative’ power rating of the converter decreases. This is because ZVS cannot be achieved when the magnetizing current is lower than the reflected load current. Hence, in order to achieve ZVS condition, magnetizing current has to be increased which increases the conduction losses due to magnetizing current in the converter and penalizes the efficiency. Therefore, an optimum value of magnetizing inductance has to be selected, to have a trade-off between the efficiency and the ‘comparative’ power rating of the converter.
- This chapter also presents the measured efficiency curves with the variation in magnetizing inductance of the transformer to show the shifting of peak efficiency point. Even though the ‘comparative’ power rating of the converter can be increased with the increase in magnetizing current, the efficiency of the converter, mainly the light load efficiency reduces due to the inevitable conduction losses from the magnetizing current.
- The converter has achieved an efficiency of 99% with low magnetizing current but the power rating of the converter has reduced to 600W. To have a trade-off between the efficiency and ‘comparative’ power rating, a reasonable value for magnetizing current has to be selected such that the light load efficiency is satisfactory. With a reasonable magnetizing current, the measured peak efficiency of the converter is 98.8% at 850W when tested up to an output power of 1 kW and has an efficiency of 98.2% at 1 kW.

5. An Optimized Bidirectional Isolated DC-DC Converter

In applications such as telecommunication, data-centers and electric vehicles, it is highly desirable to have an ultra-high efficiency bidirectional isolated dc-dc converter. The converter should be optimized to deliver power from high voltage to low voltage (buck mode) and from low voltage to high voltage (boost mode) using the same power components and to have high efficiency in almost all operating load conditions.

This chapter focuses on the bidirectional operation of an isolated dc-dc converter. The chapter starts with an introduction to the working principle of a bidirectional isolated dc-dc converter. Further, in this chapter, the loss modeling of an isolated dc-dc converter, as explained in Chapter 3, has been used to model an optimized GaN converter for an output power of 2.4 kW. The calculated efficiency curve and the power loss distribution of major power components are also discussed in this chapter.

Later in this chapter, experimental demonstration of ultra-high efficiency on a hardware prototype of a bidirectional GaN converter is presented. The measured efficiency curves for the converter in both modes of operation are also included in this chapter.

5.1. Operation of a Bidirectional Isolated DC-DC Converter

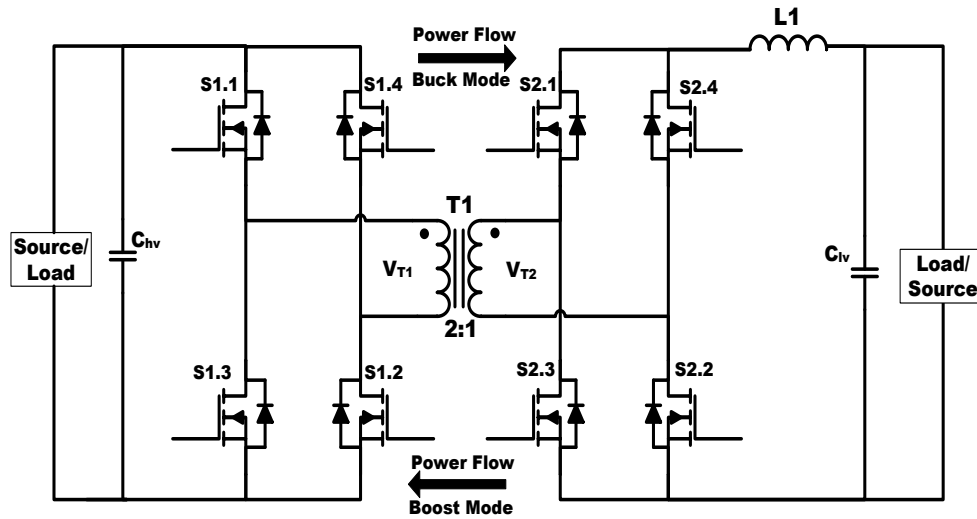


Fig. 5.1. Schematic diagram of a bidirectional isolated dc-dc converter

The circuit diagram for a bidirectional isolated full bridge dc-dc converter is shown in Fig. 5.1. The converter operates as an isolated step-down converter in forward direction (buck mode) and isolated step-up converter in backward direction (boost mode).

In boost mode of operation, the power flow of the converter is from LVS to HVS. Switches in the LVS are hard switched and operated in pairs, S2.1-S2.2 and S2.3-S2.4 respectively. The drive signals of the switch pairs, S2.1-S2.2 and S2.3-S2.4 are 180° phase shifted. Duty cycle of the LVS switches, D_d is greater than 50% to ensure continuous conduction of the inductor current.

Basic operation of the isolated boost converter can be divided into four stages,

A. Time interval between T0-T1 (Fig. 5.3)

During this interval of time, the energy will be transferred from the low voltage input to the output load. Switches S2.1 and S2.2 in the LVS and switches S1.1 and S1.2 in the HVS of the converter are conducting at this interval of time. The inductor current flows through the switch S2.1, transformer, T1, switch S1.1, output capacitor, C_{hv} , switch S1.2 and returns through the switch S2.2. During this interval, the inductor current discharges.

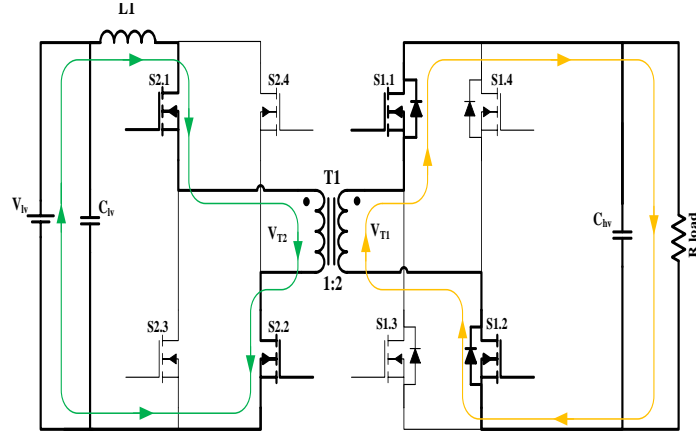


Fig. 5.3. Isolated boost converter operation: time interval between T0-T1

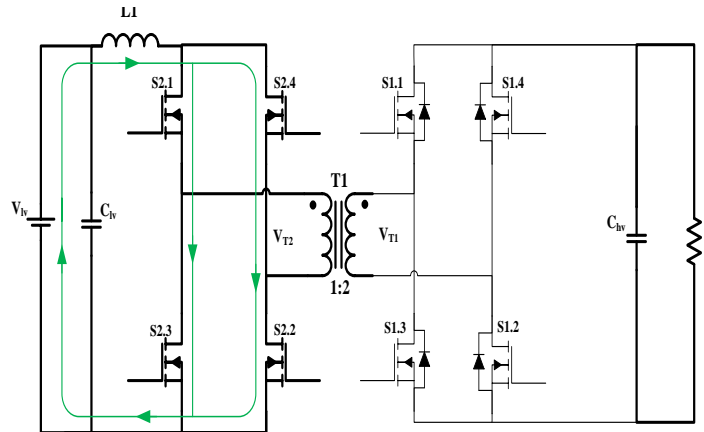


Fig. 5.4. Isolated boost converter operation: time interval between T1-T2

B. Time interval between T1-T2 (Fig. 5.3)

This period is initiated by turning-on the LVS switches S2.3 and S2.4 and turning-off the HVS switches S1.1 and S1.2. In short, all the LVS switches are conducting and the inductor current is charging with a slope V_{lv}/L_1 . All the HVS switches are turned-off during this time interval, and there will be no current flowing in the transformer windings, except the small magnetizing current in the transformer, which will be circulating in the LVS switches S2.1, and S2.3 and/or S2.2 and S2.4 and the transformer LVS winding. During this interval, the HVS capacitor, C_{hv} provides the load current. The period ends when the LVS switches S2.1 and S2.2 are turned-off.

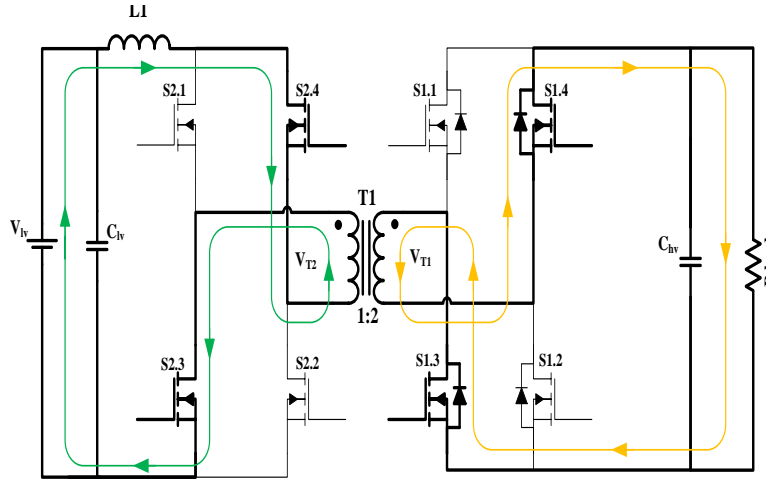


Fig. 5.5. Isolated boost converter operation: time interval between T2-T3

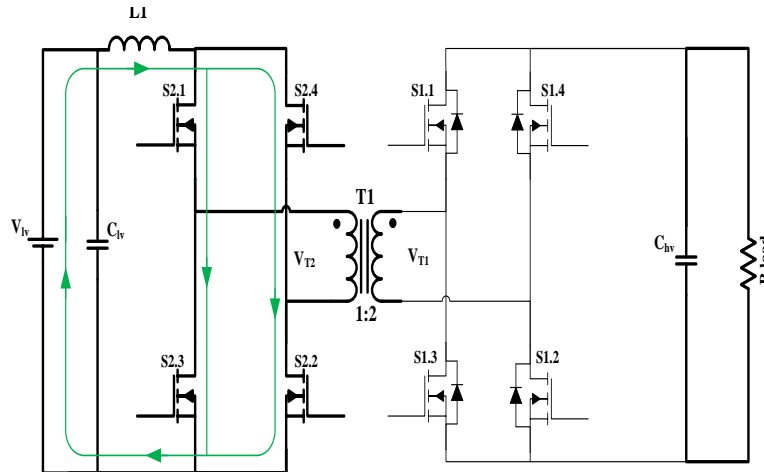


Fig. 5.6. Isolated boost converter operation: time interval between T3-T4

C. Time interval between T2-T3 (Fig. 5.5)

This period is also the energy transfer interval similar to the time interval between T0-T1. The inductor current flows through the LVS switch S2.4, transformer, T1, HVS switch S1.4, capacitor, C_{hv} , S1.3 and return through the LVS switch S2.3. This period ends when the switches S2.1 and S2.2 are turned-on and switches S1.4 and S1.3 are turned-off.

D. Time interval between T3-T4 (Fig. 5.6)

Similar to time interval between T1-T2, this interval is also an inductor-charging period. The inductor current is shared between the two parallel branches, S2.1-S2.3 and S2.4-S2.2. All the switches in the HVS are turned off during this interval.

The continuous steady state voltage transfer function of the isolated full bridge boost converter is given by

$$\frac{V_o}{V_{in}} = \frac{n}{2(1 - D_d)} \quad (5.2)$$

where, $D_d = 1 - D_c$

5.2. Converter Design

The specification of an isolated dc-dc converter for an output power of 2.4 kW is presented in Table 5.1.

Table 5.1: Converter specification for 2.4 kW output power

Output Power	P_o	2.4 kW
HVS Voltage	V_{hv}	130 V
LVS Voltage	V_{lv}	50 V
Switching Frequency	f_{sw}	50 kHz
Transformer Turns Ratio	$n:1$	2:1

Except the layout change for the GaN FETs, all the other components used for realizing the isolated dc-dc converter remains the same as given in chapter 3.

The placement of four parallel FETs on the PCB is as mentioned in Layout 2 (Fig. 3.16). The drive layout is also modified to provide proper shielding to the gate drive circuit to avoid any noise injection at the gate of GaN FETs. The parasitic inductance in the whole converter is also reduced as much as possible to avoid any voltage spikes at the GaN FETs. Even though GaN switches have low charges compared to alternative Si MOSFET, the fast transient current during each switching instant can cause ringing in the circuit. In order to reduce the parasitic

inductance, ground and power planes or traces as well as the bypass capacitors are placed as close as possible to the GaN FETs. In half bridge configuration, the connection between the top and bottom switches (i.e., high side and low side switches) is also maintained very short by keeping them back to back on the PCB.

The components used for realizing the 2.4 kW GaN converter are summarized and given in Table 5.2.

Table 5.2: Components used for realizing a 2.4 kW GaN converter

Transformer core	EE55/28
Transformer winding turns in HVS	12 turns
Transformer winding turns in LVS	6 turns
Inductor core	Kool M μ EE40
HVS switches	EPC2010C (4 devices in parallel)
LVS switches	EPC2001C (4 devices in parallel)
Driver IC	LM5114
Input filter capacitors	250V MLCC
Output filter capacitors	100V MLCC

One of the concerns in an isolated dc-dc converter is the voltage ringing at the rectifier switches. The ringing is caused by the resonance between the leakage inductance of the transformer and the output capacitance of the rectifier switches. Large leakage inductance in the transformer leads to a high leakage energy, which will increase the voltage stress at the switches used at the current fed side of the converter. This in turn, leads to use switches with higher voltage rating and hence, the conduction losses from the switches will increase at a quadratic rate [58].

Even though the leakage inductance of the transformer used for the proposed converter is extremely small, a snubber circuit is still required to reduce the voltage spike at the rectifier switches from exceeding the desired value. The energy lost at the snubber circuit can be recovered using an active energy recovery circuit [A6].

5.3. Loss Modelling for a 2.4 kW GaN Converter

The loss modelling for the proposed 2.4 kW GaN converter, as explained in chapter 3 has been carried out. The total power loss in the converter can be expressed by a second order quadratic equation, as a function of output current, I_o . (Same as equation 3.39)

$$P_{tot} = 6.81 + 0.0098 I_o + 0.0117 I_o^2 \quad (5.3)$$

From the above expression, the efficiency curve for the converter is plotted and presented in Fig. 5.7. The power loss due to the major components in the converter, namely inductor, transformer and GaN devices are also calculated [A7]. In Fig. 5.7, the area under each color shows the reduction in efficiency by these major power components in the converter.

From the loss modelling, it can be observed that the idle loss and the resistive loss contribute to the major portion of the total power loss in an isolated dc-dc converter using synchronous rectification. Idle loss determines the light load efficiency of the converter whereas the full load efficiency is determined by the resistive losses. Idle losses include the core loss from the magnetics and the capacitive losses. These losses are more dependent on the switching frequency and the input voltage. Resistive losses, on the other hand depend on the ac-resistance of the magnetics and the on-resistance of the devices. Paralleling of the device helps in reducing the resistive losses in the converter and increases the full load efficiency but this may penalize the light load efficiency. So, a trade-off between the idle loss and resistive loss is required to realize an isolated dc-dc converter to have high efficiency at both light load and full load operating conditions.

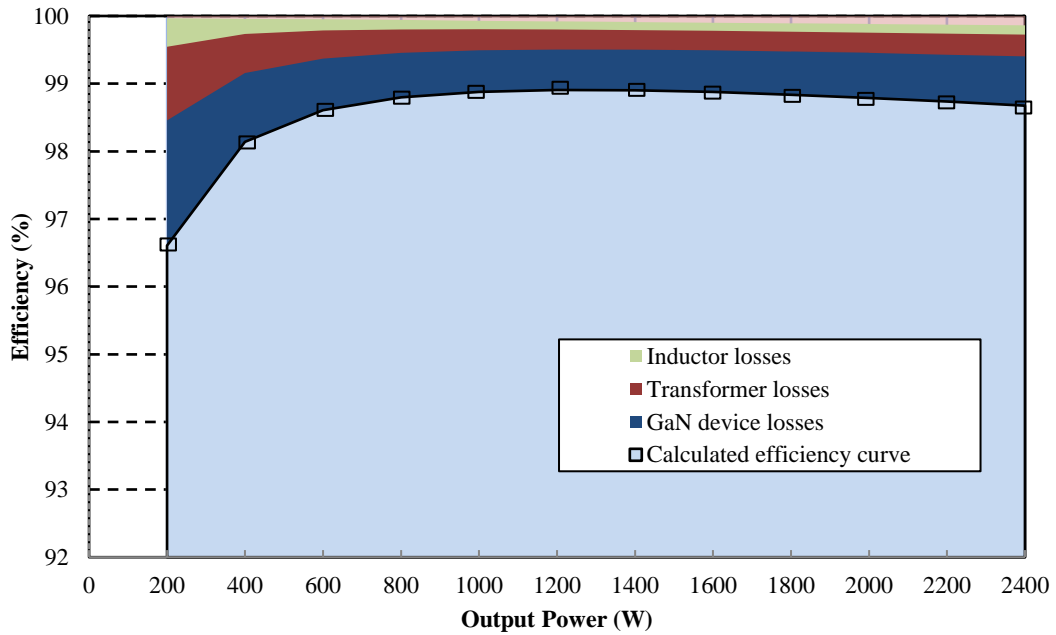


Fig. 5.7. Calculated efficiency curve of the converter showing the contribution of major loss components

The loss distribution of the converter at full load is shown in Fig. 5.8. From the loss distribution curve, it is can be concluded that when the power rating of the converter increases, the percentage of capacitive switching loss has tremendously decreased. The capacitive loss in the converter corresponds to only 0.14% of the total output power. Compared to any ZVS phase shifted converter, which uses leakage inductance to provide ZVS, will still have some switching losses. Further it also penalizes the efficiency at high output power, due to the conduction losses

in the HV switches during the freewheeling period. However, in the proposed switching pattern, all the switches at the HV side are tuned-off during freewheeling interval, so there will not be any conduction losses at the HV side during this period.

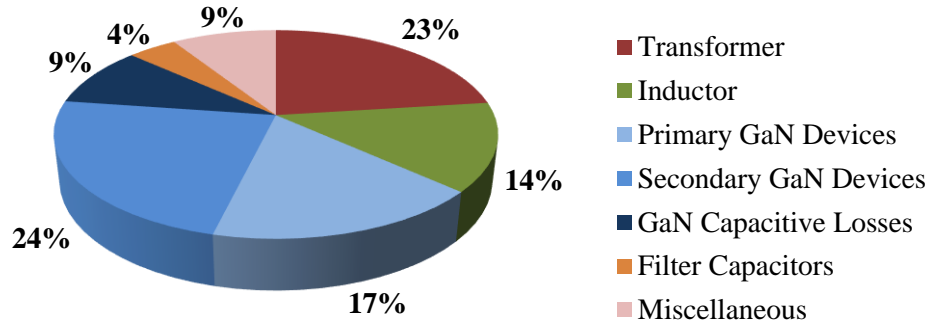


Fig. 5.8. Loss breakdown for an isolated dc-dc converter at 2.4 kW output power

5.4. Experimental Results

The hardware prototype of the proposed 2.4 kW GaN converter is shown in Fig. 5.9.

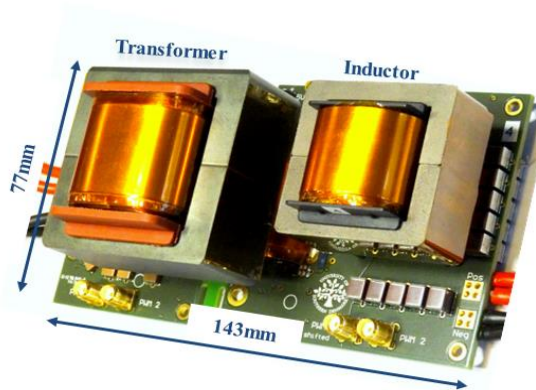


Fig. 5.9. Hardware prototype of a 2.4 kW isolated bidirectional dc-dc converter

The placement of the parallel GaN FETs for the proposed converter is shown in Fig. 5.10.

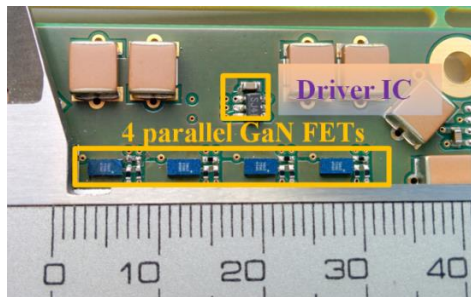


Fig. 5.10. Placement of 4 parallel GaN FETs for the proposed 2.4 kW GaN converter

The experimental results from the converter in both modes of operation are discussed below.

(a) Buck mode of operation

A dc voltage source with a voltage of 130V is connected with the HVS of the converter and the output side is connected with an electronic load. The measured waveforms of the converter are shown in Fig. 5.11. The measured waveform has no much ringing or overshoot, this itself shows that the converter is designed with very low parasitic impedance.

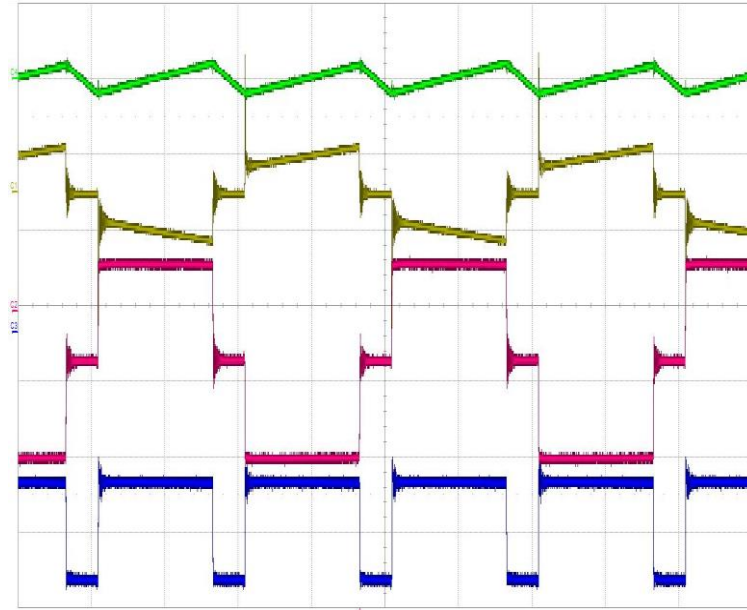


Fig. 5.11. Measured waveforms of the isolated full-bridge GaN converter (buck mode) (Green: Inductor current 20A/div, Yellow: Transformer secondary current 20A/div, Red: Transformer secondary voltage 100V/div, Blue: Voltage across Inductor 50V/div, Time: 5 μ S/div)

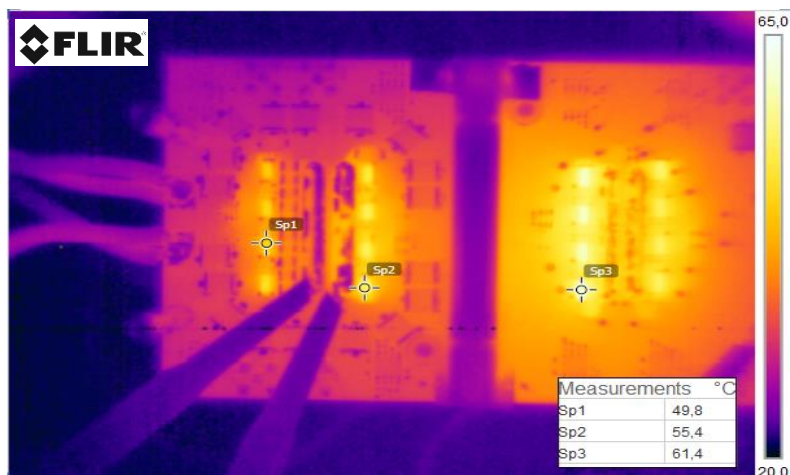


Fig. 5.12. IR image of the GaN converter at 2.3 kW of output power (buck mode)

As discussed earlier, it is almost impossible to measure the current in GaN FETs, so an IR camera from FLIR with a resolution of 320 x 240 pixels is used to monitor the temperature variations on the GaN FETs. The IR image of the converter at 2.3 kW of output power is shown in Fig. 5.12. Even at 2.3 kW output power, the device temperature is only 62°C. The magnetics and the PCB acts as a good heat sink for the GaN FETs, as they are mounted directly on the PCB.

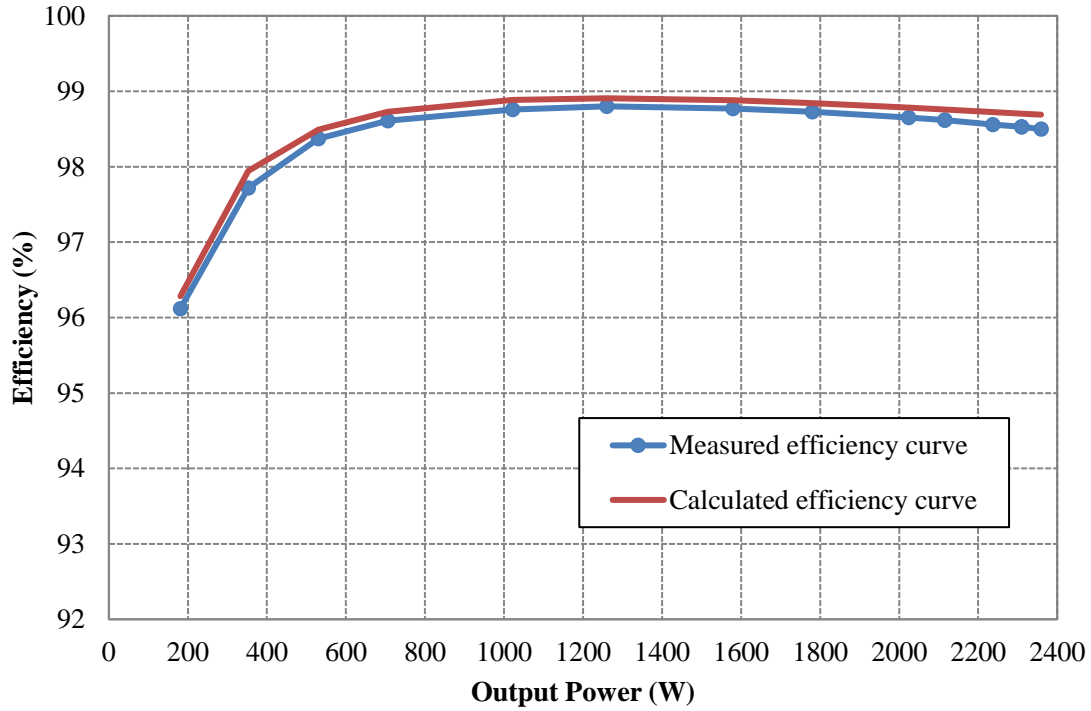


Fig. 5.13. Measured and calculated efficiency curve for the 2.4 kW isolated GaN converter (buck mode)

The efficiency of the converter is measured as explained in section 3.5 and plotted in Fig. 5.13. Measurement tolerances are less than $\pm 0.1\%$. The peak-measured efficiency of the converter in buck mode of operation is 98.8% at 1.3 kW output power. Therefore, the comparative power rating of the converter is 2.6 kW. The converter has an efficiency of above 98.5% for a wide range of output power. The flat characteristics of the efficiency curve even at light load condition confirm that the converter is optimally designed. The calculated efficiency curve of the converter from the loss modelling is also plotted in Fig. 5.13. The efficiency curve from loss modelling matches well with the measured efficiency curve. This validates that the proposed loss modelling can be used to design any isolated dc-dc converter.

(b) Boost mode of operation

In boost mode, the converter is fed with an input voltage of 50V at the LVS and an electronic load is connected at the HVS. The operational waveforms of the converter is measured and

shown in Fig. 5.14. The efficiency of the converter is measured using the same setup as explained in section 3.5. The IR image of the GaN converter is also monitored at full load using the FLIR camera and shown in Fig. 5.15. The measured efficiency curve is shown in Fig. 5.16. The measured peak efficiency of the converter in boost mode of operation is also 98.8%. The converter also has a flat efficiency characteristic and has an efficiency of above 98.5% over a wide range of output power.

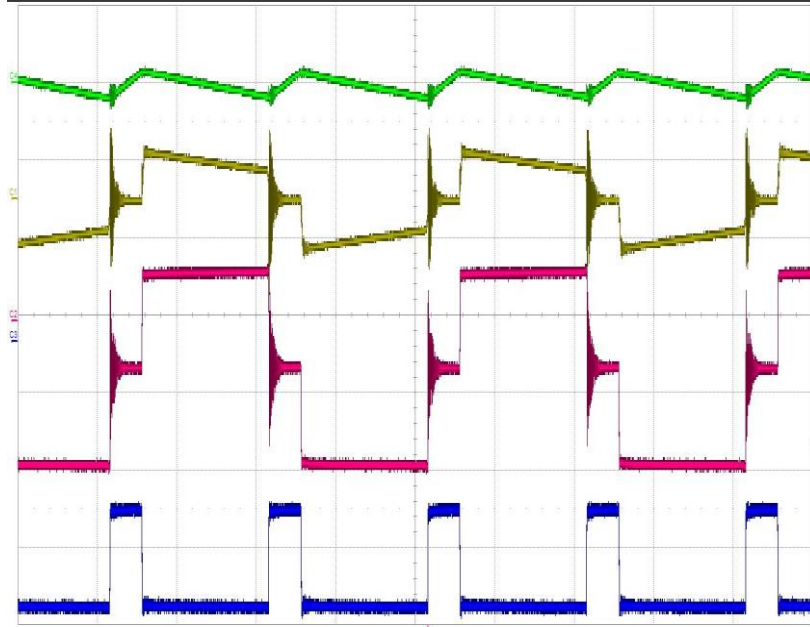


Fig. 5.14. Measured waveforms of the isolated full-bridge GaN converter (boost mode) (Green: Inductor current 20A/div, Yellow: Transformer secondary current 20A/div, Red: Transformer secondary voltage 100V/div, Blue: Voltage across Inductor 50V/div, Time: 5 μ S/div)



Fig. 5.15. IR image of the GaN converter at 2.2 kW of output power (boost mode)

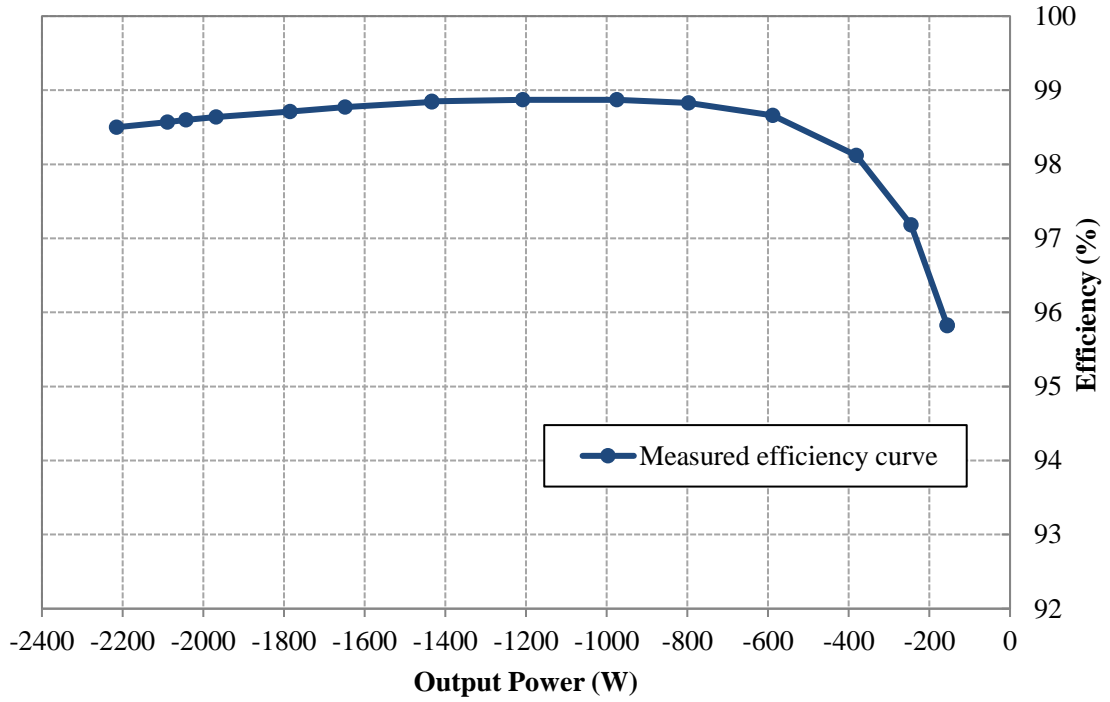


Fig. 5.16. Measured efficiency curve of the GaN converter in boost mode of operation

The converter has achieved a maximum efficiency of 98.8% in both directions of power flow. The converter also exhibited a flat efficiency curve in both directions, this concludes that the isolated dc-dc converter is optimally designed for working in both boost and buck mode with the same power components. The PCB and the magnetics acts as a sufficient heat sink for the converter. This avoids external cooling system or heat sink requirements, allowing the converter to be more compact, which in turn increases the power density of the whole converter. The power density of the proposed bidirectional converter is calculated as 7 kW/liter.

5.5. Conclusion

This chapter presents the experimental demonstration of ultra-high efficiency in an optimized bidirectional isolated dc-dc converter utilizing GaN FETs as switching devices.

- Calculated efficiency curve from loss modelling of the proposed 2.4 kW GaN converter matches well with the measured efficiency curve. This verifies that the proposed loss modelling can be used for precisely predating the conversion efficiency of an ultra-high efficiency isolated dc-dc converter. Thus, the proposed loss modelling becomes a powerful design tool.
- The increase in efficiency reduces the heat sink requirement. As PCB and the magnetics will act as the heat sink, there will be no further requirement for any external heat sinks.

- Since there is no heat sink used to realize the proposed converter, the size of the whole converter is reduced, which implies that, high power density in isolated dc-dc converter can be achieved. The power density of the proposed 2.4 kW bidirectional isolated GaN converter is 7 kW/liter.
- Optimum layout is another important criterion in an isolated dc-dc converter to achieve high efficiency. By optimizing the layout, the ‘comparative’ power rating of the converter is increased by 30%, i.e. from 2 kW in 1.7 kW GaN converter (Chapter 3) to 2.6 kW in 2.4 kW GaN converter (Chapter 5).
- Optimum layout also increases the maximum efficiency of the converter. The peak efficiency of the isolated GaN converter is increased from 98.5% in chapter 3 to 98.8% in Chapter 5, i.e. a reduction of 20% of power loss, by optimizing the layout.
- Experimental results verifies that with usage of high efficiency magnetics, GaN devices and a proper layout for an isolated dc-dc converter, bidirectional operation is possible with ultra-high efficiency in both directions of power flow. The maximum measured efficiency of the proposed converter, in both buck and boost mode of operation is 98.8%.
- The proposed bidirectional converter has exhibited an efficiency of above 98.5% from 25-85% of output power in both directions of power flow, i.e., low power loss over a wide range of operating load conditions.

6. Conclusion and Future Work

6.1. Conclusion

High conversion efficiency is invariably desirable in all power converters. The major objective of this research work was to achieve the highest possible conversion efficiency in an isolated dc-dc converter.

Due to the superior characteristics of GaN devices, they have been selected as the switching devices. GaN FETs shows at least 2 times lower output capacitive charge for a specified on-resistance, compared to an alternative Si MOSFET. This will proportionally reduce the switching losses in an isolated dc-dc converter, which will increase the light load efficiency of the converter. Compared to an alternative Si MOSFET, GaN FETs have an extremely low gate drive losses due to the small input capacitance and the low gate drive voltage. Unlike Si MOSFETs, GaN FETs does have a parasitic bipolar junction; so there will be not be any reverse recovery losses. This helps in improving the efficiency of an isolated dc-dc converter with synchronous rectification.

Optimum layout is another important factor to achieve ultra-high efficiency. Layout should be designed such that the parasitic circuit elements are reduced as much as possible. The parasitic elements in the circuit as well as in the devices has to be extremely low. Paralleling of GaN devices and optimum gate drive circuit for these FETs was one of the major challenges in this research work. Special precautions are taken to ensure proper current sharing in paralleled GaN FETs, without reducing their switching speed. Careful layout for paralleling the GaN FETs and the compact placement of filter components on the PCB helps in reducing the ac-resistance and the parasitic inductance in the converter, which will increase the switching speed of the GaN FETs, reduces the switching losses and thereby, increases the efficiency of the converter.

A capacitive loss modelling for an isolated dc-dc converter has been formulated in this thesis. For GaN FETs with a switching frequency of 50 kHz and input voltage of 130V, the capacitive switching loss in the isolated dc-dc converter is calculated as approximately 3.3 W. This contributes to 9% of the total power loss in a 2.4 kW GaN converter.

In order to reduce the capacitive switching losses, a zero voltage switching isolated dc-dc converter has been realized using the magnetizing current in the transformer. This help in reducing the switching loss even at light load condition. However, it has been analyzed and verified by experimental results that when the reflected load current is higher than the magnetizing current, soft switching ceases and the converter becomes hard switched. This will effectively reduce the ‘comparative’ power rating of the converter.

Initially, a 1.7 kW GaN converter is realized and the efficiency of the converter is measured. The maximum measured efficiency of the 1.7 kW GaN converter is 98.5%.

Later with the optimization of layout, a 2.4 kW GaN converter has been realized. The maximum measured efficiency of this converter is 98.8%.

Comparing the two converters, which uses the same power components and are rated for 1.7 kW and 2.4 kW output power respectively, the following conclusions can be made:

- The capacitive switching losses in GaN FETs contributes to 16% of total power losses at 1.7 kW output power. When the power rating of the converter was increased to 2.4 kW, with the optimization of layout, the loss percentage has reduced to 9% of the total converter losses, which corresponds to only 0.14% of the total output power.
- The maximum efficiency of the converter has been increased from 98.5% in the 1.7 kW converter to 98.8% in the 2.4 kW GaN converter; in other words, a power loss reduction of 20% has been achieved with the optimization of layout.
- With the optimization of layout, the ‘comparative’ power rating of the converter has increased from 2 kW to 2.6 kW for 1.7 kW and 2.4 kW GaN converter, respectively; in short, the ‘comparative’ power rating of the converter has increased by 30%, only by optimizing efficiency through improved layout.

A complete analytical loss modelling of the isolated dc-dc converter is also presented in this thesis. The measured efficiency curve of the 2.4 kW GaN converter matches well with the calculated efficiency curve from the loss modelling. This validates that the proposed loss modelling can be used to precisely predict the conversion efficiency of an ultra-high efficiency isolated dc-dc converter and thus becoming a very powerful design tool.

The optimized 2.4 kW isolated dc-dc converter is tested for bi-directional operation and the converter has achieved a maximum measured efficiency of 98.8% in both directions of power flow. The converter has also attained an efficiency of above 98.5% from 25 - 85% of the output power. This gives a flat efficiency curve in both directions, which implies low losses over a wide range of operating load conditions.

An ultra-high conversion efficiency of 98.8% in an isolated bidirectional dc-dc converter has been experimentally demonstrated and analytically verified in this research work.

6.2. Future Work

A complete controller for the GaN converter with voltage and current control, protection circuit will need to be designed and developed to meet various requirements specified by the various applications.

Recently some 600V GaN devices are commercially introduced; a converter designed with these high voltage GaN devices will be highly needed and attractive in many applications such as telecom, electric vehicles, and renewable energy applications.

Even though the converter specified in this thesis uses very high efficiency magnetics, the accurate measurement of individual losses in these magnetics, both core loss and copper loss are still challenging, so a better model for the magnetics has to be developed and a precise measurement of these losses has to be demonstrated.

An isolated dc-dc GaN converter with a switching frequency of 100 kHz or above will need to be designed and developed to demonstrate the relation between the size of the converter and the conversation efficiency.

GaN FETs switches much faster than conventional Si MOSFET, so a detailed study on EMI and EMC issues and the design of common mode filters for the GaN converter will need to be further investigated

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Appendix A

Appendix A contains the list of papers published as a part of this project.

- A1. R. Ramachandran, M. Nymand, N.H. Petersen, "Design of a compact, ultra - high efficient isolated DC-DC converter utilizing GaN devices," in *Proc. of the Annual Conference of the IEEE Industrial Electronics Society, IECON 2014*, pp. 4256-4261, Oct/Nov 2014.
- A2. R. Ramachandran, M. Nymand, "Design and Analysis of an Ultra-High Efficiency Phase Shifted Full Bridge GaN Converter," in *Proc. of the Applied Power Electronics Conference and Exposition (APEC 2015)*, pp. 2011-2016, Mar 2015.
- A3. R. Ramachandran, M. Nymand, "Switching losses in a 1.7 kW GaN based full-bridge DC-DC converter with synchronous rectification," in *Proc. of the European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1-10, Sept 2015.
- A4. R. Ramachandran, M. Nymand, "Analysis of capacitive losses in GaN devices for an isolated full bridge DC-DC converter," in *Proc. of the International Conference on Power Electronics and Drive Systems (PEDS 2015)*, pp. 467-472, Jun 2015.
- A5. R. Ramachandran, M. Nymand, "A 98.8% Efficient Bidirectional Full-Bridge Isolated DC-DC GaN Converter," in *Proc. of the Applied Power Electronics Conference and Exposition (APEC 2016)*, pp. 609-614, Mar 2016.
- A6. R. Ramachandran, M. Nymand, "An Energy Recovery Clamp Circuit for an Isolated DC-DC GaN Converter," in *Proc. of the International Telecommunications Energy Conference (INTELEC 2016)*, accepted for publication.
- A7. R. Ramachandran, M. Nymand, "Experimental Demonstration of a 98.8% Efficient Isolated DC-DC GaN Converter," *IEEE Trans. Ind. Electron*, accepted for publication.

Appendix A1

R. Ramachandran, M. Nymand, N.H. Petersen, "Design of a compact, ultra -high efficient isolated DC-DC converter utilizing GaN devices," in *Proc. of the Annual Conference of the IEEE Industrial Electronics Society, IECON 2014*, pp. 4256-4261, Oct/Nov 2014.

Appendix A2

R. Ramachandran, M. Nymand, “Design and Analysis of an Ultra-High Efficiency Phase Shifted Full Bridge GaN Converter,” in *Proc. of the Applied Power Electronics Conference and Exposition (APEC 2015)*, pp. 2011-2016, Mar 2015.

Appendix A3

R. Ramachandran, M. Nymand, "Switching losses in a 1.7 kW GaN based full-bridge DC-DC converter with synchronous rectification," in *Proc. of the European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1-10, Sept 2015.

Appendix A4

R. Ramachandran, M. Nymand, “Analysis of capacitive losses in GaN devices for an isolated full bridge DC-DC converter,” in *Proc. of the International Conference on Power Electronics and Drive Systems (PEDS 2015)*, pp. 467-472, Jun 2015.

Appendix A5

R. Ramachandran, M. Nymand, “A 98.8% Efficient Bidirectional Full-Bridge Isolated DC-DC GaN Converter,” in *Proc. of the Applied Power Electronics Conference and Exposition (APEC 2016)*, pp. 609-614, Mar 2016.

Appendix A6

R. Ramachandran, M. Nymand, “An Energy Recovery Clamp Circuit for an Isolated DC-DC GaN Converter,” in *Proc. of the International Telecommunications Energy Conference (INTELEC 2016)*, accepted for publication.

Appendix A7

R. Ramachandran, M. Nymand, “Experimental Demonstration of a 98.8% Efficient Isolated DC-DC GaN Converter,” *IEEE Trans. Ind. Electron.*, accepted for publication.